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JUNE 2018

PCB007 MAGAZINE

Wet Processing Trends 2018


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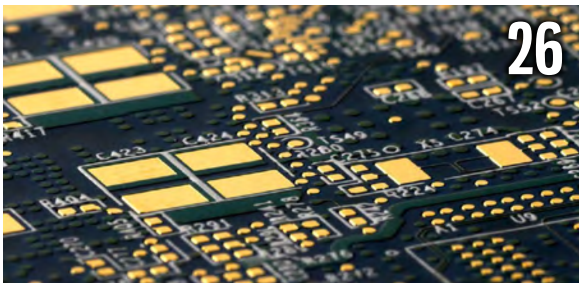
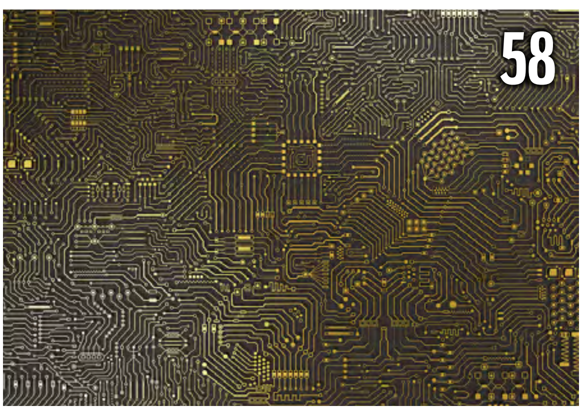




Wet Processing Trends 2018

Much like the ubiquitous rubber ducky, it seems that PCB manufacturing has not changed much through the decades, but what *has* changed is the required precision of those steps to achieve ever finer features at ever higher levels of quality and reliability. This month, our experts offer up new wet processes, and tips and best practices for successful plating, and more.

PCB007 MAGAZINE

COLUMNS:

HIGHLIGHTS:

SHORTS:

DEPARTMENTS:

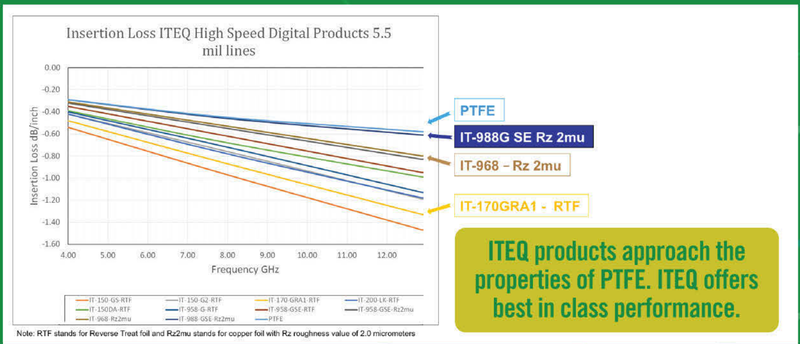
IT-968 / IT-968 SE

High Thermal Reliability
Designed for High Speed Digital Applications
- Telecom, Backplane, Base Station, Server, Storage, Switch

IT-968
Dk @ 10 GHz - 3.66
Df @ 10 GHz - 0.005

IT-968 SE
Dk @ 10 GHz - 3.16
Df @ 10 GHz - 0.0037

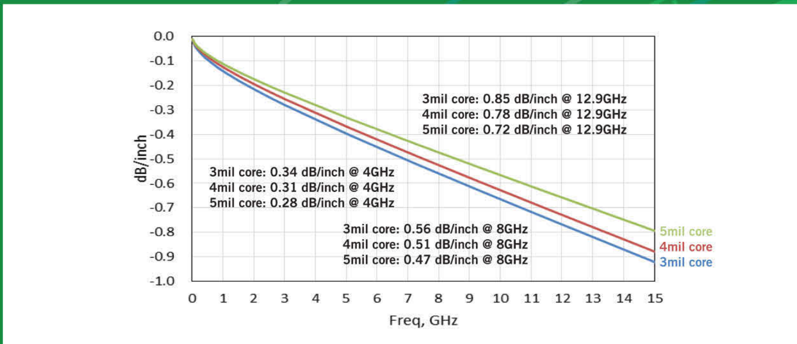
Insertion Loss - Measured



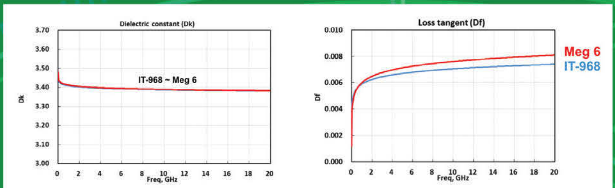
Industry Test Vehicle

32 layers, 0.140" thick
Four 2 oz copper internal layers
0.8 mm pitch, 9.8 mil drills
- Passed 1000 hours CAF, 10 V bias, 50 V
- IST - Passed 1000 cycles, 6x 260°C precondition
- No delamination after 8x 260°C reflow after 2 weeks at 35°C/ 85 % RH

IT-968 Loss Performance



IT-968 SPP Comparison



GHz	10		12.9		16		20	
Parameter	Df	Dk	Df	Dk	Df	Dk	Df	Dk
IT-968	0.0071	3.39	0.0072	3.39	0.0073	3.38	0.0074	3.38
M6	0.0076	3.39	0.0078	3.39	0.0079	3.38	0.0081	3.38
%	7.95	0.04	8.52	0.04	8.98	0.03	9.45	0.02

Ultra Low Loss IT-968 SE

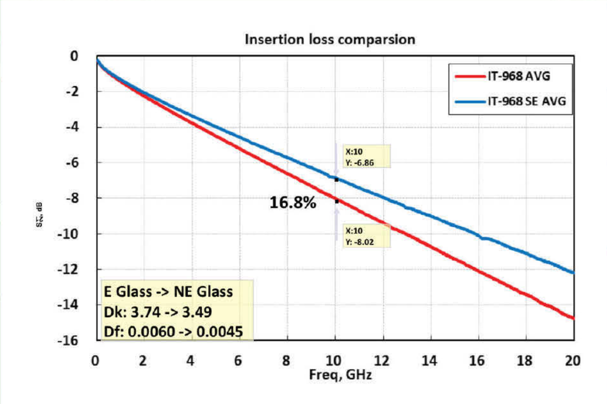
Features
High Tg, low CTE, High Thermal Reliability with Ultra Low Df < .005. Designed for High Speed Applications.

Applications
Server/Storage/Switch (10G/40G/100G), Backplane, Telecom, Base Station

Feature *High Speed , 25Gbs/path Solution*

Property	Test Method	IT-968	IT-968 SE
Tg (℃)	DSC	185	185
T-288 (w/ 1 Oz Cu, min)	TMA	120+	120+
Td-5%(℃)	TGA 5% loss	390+	390+
CTE (%), 50-260℃	TMA	2.2	2.2
Peel strength (lb/inch)	1 oz	6	6
Water Absorption	D-24/23	< 0.1	< 0.1
Dk , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	3.8 3.8-3.7	3.4 3.4-3.3
Df , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	0.0032 0.0038-0.0050	0.0028 0.0031-0.0040

E-Glass vs Low Dk Glass



ITEQ

Staying Current on Wet Processes

Patty's Perspective

by Patty Goldman, I-CONNECT007

I live in Pennsylvania, in a town of 4,000 people, and I can walk to the library, grocery, post office, and a couple of restaurants and always meet someone I know. Running into people I know at the farmer's market and drugstore was something of a shock to me when I first moved here but I enjoy it quite a bit.

I'm writing this a few days after our Memorial Day parade, which consisted of two bands, the local veterans organizations (French & Indian and Civil Wars are especially studied around here), several parade floats, a number of county and town officials in cars (including Miss Pennsylvania), and best of all, numerous fire trucks and emergency vehicles. I can count 11 or 12 volunteer fire companies within a 5–7-mile radius of this little town—and that's nowhere near the whole county. I'm a big fan of volunteering, so I find this kind of thing heartening, as I do with the fact that our recent Day of Giving raised almost $340,000 for local charitable organizations. If you don't have this where you live…move! And let me move on now to our topic for this month.

Figure 1: A small contingent of the award-winning Kittanning Firemen's Band marching on Memorial Day (one doesn't have to be a volunteer fireman to be in the band).

My undergraduate degree is in chemistry (a zillion years ago) so the PCB wet processing area was a natural for me. Ah, the smell of ammonia and formaldehyde and acids! The beauty of an automatic plating line and the preciseness of a well-synchronized conveyorized DES line! The sense of triumph when we actually processed thousands of innerlayers with 5 mil line and space—in the early '80s—successfully and with high yields (yeah, manual inspection). Of course, I haven't worked in a PCB facility for quite a while now, having branched off into marketing, sales and R&D as well as other parts of the process. And now, "I are an editor!" (How did that happen?)

But, back to wet processing. More than one of our writers has said the PCB manufacturing has not changed much—and in a sense that's true. There are still the myriad steps: image, etch, strip, laminate, drill, PTH, image, electroplate, strip and etch—or some variation of these. What has changed significantly is the required precision of those steps to achieve ever finer features at ever higher quality and reliability on ever more persnickety materials for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Scrubbers
Developers
PTH
Oxide Replacement
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ever more demanding customers in ever shorter time spans at ever lower costs and prices. How the heck do PCB companies accomplish this?

Not alone, of course. The suppliers of both chemistry and equipment have been hard at work to help their PCB customers keep ahead of the curve. Much improved chemistry with better process windows, more reliable control, and lower toxicity have been at the forefront. And much research and improvement have gone into equipment in the form of both automation and—shall we say—efforts at process consistency (think spray and pump technology). So, let's look at what these people have to say and hopefully you will pick up some pointers and tidbits and learn about some new processes at the same time.

To put everything in perspective, we turned to specialty chemical company MacDermid Enthone (yours truly worked for two of the original companies). Don Cullen, Jordan Kologe and Ted Antonellis filled us in on not just what's new in chemistry but also in analysis and automation.

Lately, one of the areas of concern for both PCB manufacturers and their customers is the final finish on the PCB—and the greatest of these seems to be in the ENIG, ENEPIG, etc., types. Atotech's Rick Nichols next presents an article on autocatalytic gold—as opposed to immersion gold—as a final finish being championed by the automotive industry for its high reliability.

Coming at it from the equipment side of things is Viking's Marc Ladle with an interesting article on how changes in equipment design can have a profound effect on the chemistry. I think suppliers on both sides will tell you how important it is that they work together.

Our next article comes from Uyemura, in Japan. Tetsuya Sasamura and colleagues address a different final finish, this one without nickel—a gold/palladium/gold process. According to the article, it is very good for extremely fine features.

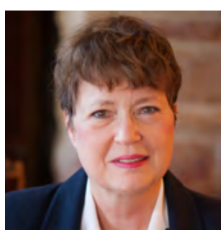
Another recent area of concern is via filling and we have an article by Saminda (Sam) Dharmarathna, et al., of MacDermid Enthone, on an electroplated via fill process which looks most interesting. This process can electroplate copper in a via while keeping the surface copper thin—quite a trick!

This month, Mike Carano's "Trouble in Your Tank" column on troubleshooting PTH failure mechanisms fit well with our wet processing topic. We hope you benefit from his practical knowledge and are storing his columns for future reference!

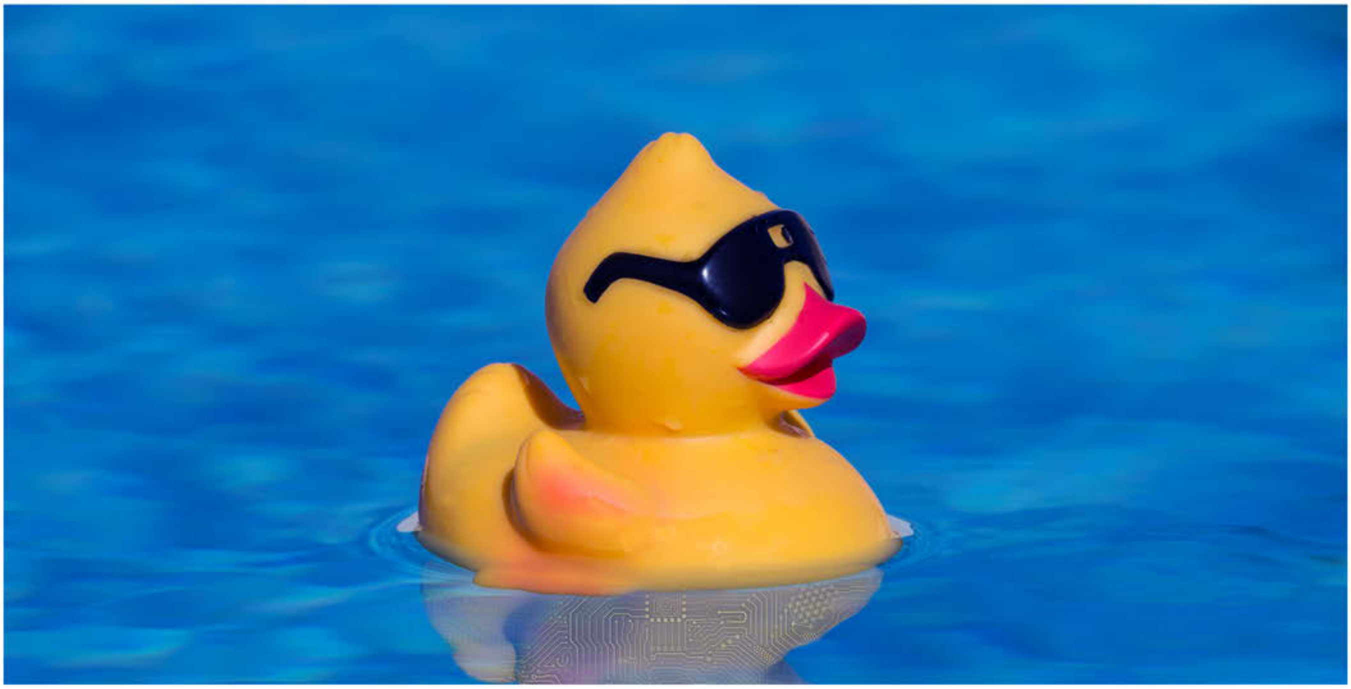
Our final column this month comes from Elmatica's Didrick Beck. The subject is Lean manufacturing and the differences between standard and non-standard product lines. Good information to know.

OK, so some of these articles have a lot of charts and graphs, and data that may seem daunting, but the information is worth reading so don't skip over them.

Finally, getting back to volunteering, I'm looking forward in the months ahead to doing more local volunteering at our library, the historical museum, the animal shelter, and of course gardening. We are already moving one of our editors into the role of shepherding our columnists (interested in writing for us?) and I'm backing off on more editorial duties to free up some time. Not gone, just moving aside a bit to get into some other interests, so keep on reading and I will see you next month when we fill you in on the latest in solder mask technology. You are subscribed right? (Gotta ask!) **PCB007**



Patricia Goldman is managing editor of *PCB007 Magazine.* To contact Goldman, click here.



MacDermid Enthone Talks Wet Processing Trends in 2018

Feature by the I-Connect007 Editorial Team

I-Connect007's Patty Goldman, Barry Matties, Andy Shaughnessy, and Happy Holden were recently joined by MacDermid Enthone team members Jordan Kologe, technical marketing specialist; Ted Antonellis, applications manager for electronics specialties; and Don Cullen, marketing director for electronics solutions and MacDermid performance solutions. The discussion topic was the wet processing end of PCB manufacturing.

Patty Goldman: We're here to talk about wet processing for PCB manufacturing. What do we need our readers to know about wet processes?

Don Cullen: We just got back from some customer roadmap sessions in China, Thailand, Taiwan, Singapore, Korea, Hong Kong. A couple of the themes that are going through my head include the transition of automotive circuitry to finally adopting HDI and microvia designs. It is kind of surprising they hadn't really done it yet, but that seems to be happening this year. Also, there's a big theme around circuit boards becoming more like IC substrates and IC substrates trying to emulate the cost and productivity advantages of circuit boards. We're all trying to marry up the technology and fine line/fine pitch metrics between wafers, IC substrates, and bare PCBs. It all affects the trends in SAP and modified SAP technology.

Barry Matties: From the applications engineer point of view, what challenges are they looking to solve that's currently in place?

Ted Antonellis: We support a lot of different processes. I spend most of my time in bonding chemistry, the alternative oxides. People want smoother and smoother coppers for signal integrity, so there are newer processes that depend more on chemical bonding than the actual mechanical bonding to improve on that. Aside from that, in some of the other circuit for-

mation areas, there's not a whole lot of change. My team supports resist strippers and tin strippers and those types of chemistries as well.

Matties: Do you see any desire for a zero-discharge facility and is that coming into play as we see at Whelen?

Antonellis: I think Whelen is the only one that I know of in full use of that concept.

Cullen: Many customers talk about zero discharge. It has not really been happening. I did hear about some new legislation in China that's coming down the pike for facilities within a certain distance of the protected rivers, five kilometers or something like that. It was going to be zero discharge, so a couple of the guys I spoke to said that they would have to close facilities, and I hadn't heard of that before. I've heard companies applying for permits in different areas based on the restrictions, but there was going to be closure of some significant facilities. As far as I know, it hasn't happened yet, but I've heard the rules are on the way.


Don Cullen

Matties: It's counterintuitive to China, isn't it?

Cullen: Well, in a historic perspective yes, but we've seen that China has gotten much stricter than even some of the European and North American standards. It started with phosphorus and then it came down to metals and chelators. Now it's just zero, no effluent. Cyanide, of course, hit China's platers hard. After a big set of explosions in East China a couple of years ago, and then the algae blooms in lakes outside Shanghai, the smog control measures during high-profile events like the G7 meetings and the Olympics, it seems like serious environmental change in China is really happening now.

Goldman: That's interesting. It's almost like a backlash. The pendulum swings further to the other side than you might think it should or would.

Cullen: It really has. In my view, they might be rushing into new regulations a bit too quickly.

Matties: What sort of automated control systems are you seeing, and what are the advantages?

Antonellis: I don't see much besides specific gravity controllers that might be on a machine. And then there is always a manual analysis that's happening back in the lab to confirm any adds that were made automatically. There are nickel controllers for ENIG and electroless copper always has controls, and CVS is used quite a bit for electrolytic plating baths.

Matties: I would think with IoT and the surge of sensors everywhere that we would be seeing this in our plating departments. Is there not a desire, or is it not needed, or is there just not enough efficiency to be gained?

Jordan Kologe: Part of what we do here is come up with innovative processes that simplify different manufacturing steps. A lot of our work is focused on coming out with products that can combine manufacturing processes into the same step. I'm sure a lot of companies are heading down that road as they try to get higher yields. They're trying to reduce the number of opportunities for defects going through a line, that sort of thing.

Cullen: I'm sure you're right, Barry. The IoT revolution is going to enable a lot more automated control. We see this more in our industrial or metal finishing business. That, again, is a little bit counterintuitive, because many metal finishing shops don't have the sophisticated laboratories and a lot of the engineers running around like the circuit fab shops do. So metal finishing shops can tend to have more automation and cloud data sharing. We also see more sophisticated automated process control at IC substrate or wafer manufacturing.

But for the metal finishing guys, we offer a program which they install. It involves controllers and software that can be accessed securely online, where we can go in and check on their SPC and make recommendations. PCB manufacturers, by contrast, for the most part, they have their equipment, they have their people, they have the double-checking, and not a ton of automated analysis and replenishing. A lot of the replenishment is just done on a per-square-foot basis.

They have the metering pumps on the drums of chemicals; a light sensor will detect the board going into a process, and then when it has counted five boards, it pumps X milliliters into the bath, something like that. That's probably the most common. Electroless controllers are widely deployed for most, but the rest of the baths, I think it's just per board.

Matties: What about in the equipment area? Are you seeing changes in equipment to meet the new needs based on your baths that are coming in, your chemicals?

Kologe: For high tech, it is about customization, for mid-range tech it is about compatibility. There are certain processes that we release for advanced technology that are highly customized, and the equipment needs to be from an approved supplier. On the opposite side of the spectrum, a lot of the baths that we sell, even though they are specialty processes, they still are installable in existing lines. That's one of the things that our customers look for in a lot of the mid-range technology chemistry.

Cullen: There are a couple of outliers on that. For example, the big vertical platers for plating vias and filling vias—those are still kind of tightly controlled in the supplier of the equipment. We have great relationships with the guys who make these big vertical platers, and I guess over time that's going to commoditize just like everything else. You know the difference with horizontal electroless, a lot of that market has been locked down to equipment specification. We are installing some horizontal electroless now with other equipment suppliers, so that is starting, again, to commoditize.

The equipment that's arriving now for through-hole filling is extremely controlled, and it's not widely deployed yet, but for our customers who do that, we write the equipment specification and it's built exactly to our standards. That's kind of the other extreme of the equipment relationship. I've got a lot of cases from the photovoltaics (PV) industry, but not so many examples in circuit boards right now. Maybe a good example of chemistry/equipment design coordination is in the handling of small parts and thin materials for flex.

Matties: When people look at their wet process, are they looking at it from a cycle time point of view as well, or are they coming in saying not just cycle time, but even process step elimination?

Kologe: For cycle time, in electroplating processes, for example, you just scale up the tank if you want to have higher throughput. Even if the cycle time is longer, if they are willing to install a larger line in their factory that can handle the amount of throughput, then the cycle time is kind of a non-issue.

Cullen: That's always the thing. Jordan is talking about making sure there's no rate-limiting step. If there's one step that takes much longer and it's out of sync, then they'll make that one

step more capable. An example is the smartphone boards we plate at some of these big Asian shops; they have dozens of these giant vertical continuous platers, so yeah, cycle time to them is a big deal, because every new line is multi-million-dollar CapEx. It is a big deal if we can trim time off, and we do that. There's a continuous drive. I think this fits exactly in with your theme.

Kologe: There's also a constant push to bump up our current densities. Whether it's strict DC or it's pulse plating for high aspect ratio, everything we can do to reduce that cycle time. Just like you said, Barry, there are a couple of places where we have been able to take two processes and turn it into one. We have this product we featured at IPC APEX EXPO, the VF-TH, which is via filling conformal through-hole plating of electroless copper in one step instead of doing the filling with a mask, stripping that, imaging it, and then doing the conformal plating. Now it's one bath, so that's a huge value proposition right there.

Jordan Kologe

Matties: I think people will jump on that, because you're also reducing the chance for failure as well by eliminating steps.

Cullen: That's 100% right. That's another thing that came out of the technology roadmap sessions. They were technology sessions, but the guys kept coming back saying, "If I have five steps and you guys are happy to advertise that your defect rate is 0.05 ppm or whatever, but you know, in my circuit board shop I've got 150 steps and you start adding all those up and if I have a couple of steps that are a little bit out of whack, I get 20% failure." There are some big, new investments for high-tech IC substrates, and they are not running profitably right now because their defect rate is 25–30%. So they don't care so much about adopting new technology. They're obsessed with reducing defect rates on every single process step.

Matties: That's got to be the priority. Eliminate defects and then focus on throughput speeds.

Cullen: But then, at the same time, they're challenged because Apple and Samsung come in and say, "Oh, now you're going to build to this even tinier micron line/space." So in that case, they've got to adopt new processes, and new processes have high defects, right? But if they don't do it, they drop out of the supply chain.

Matties: With HDI coming into the automotive space—I think the stat is by 2020, 50% of the value of the cars is going to be electronics—what challenges are you seeing?

Cullen: Frankly, I think that the adoption of HDI into automotive is slow just because of fear, not because of reality. They're going to get much better circuitry when they deploy it, right?

Happy Holden: Well, we've been covering up the problem, but we have a massive problem in HDI reliability on military boards, and a lot of my time at IPC APEX EXPO was spent on this. Frankly, it's a dilemma that the processes aren't optimized. We're not sure that we are using the right design rules. We seem to have a problem with a spongy electroless. We're seeing a lot of failure of stacked vias, things like that, with one set of vias delaminating from the plating underneath it right at the electroless line.

Cullen: Yes, Happy, I've seen some of this on circuitry blogs, and posts that have been forwarded to me, and I can speculate on this. We do continuously push HDI manufacturers to a direct metallization to remove that extra layer of copper between the foil copper and the plated copper. Even the direct metallization systems now are including ways to prevent the direct metallization of material, like the carbon

or the graphite or the conductive polymer from sticking to the copper in the first place, so it's always just a plated copper in intimate contact with foil or other plated copper. It's a copper-to-copper interface. That's one thing. The simplicity of the direct metallization avoids the complexity of electroless copper systems. And it's only when electroless copper is operated incorrectly that failures occur.

The other thing is the expansion in Asia. They took advantage of all the new modern designed equipment that has been installed over the last 10 years. In North America, we still see a lot of attention to retrofitting equipment that's been around for decades. That is a problem for sure. It's like my telephone service stinks because it was built in 1940, but if you go to Southeast Asia, their telephone equipment was built 15 years ago, and it's awesome. It's a bit of that challenge working with first-generation technology.

Holden: It is. Have you had a chance to see Alex Stepinski's information on zero discharge and recycling? One of the things he does is elevate the temperature of a lot of critical baths, and then he uses a stagnant dragout followed by a high flowing cascade rinse. He hermetically sealed machines full of negative pressure. Then, he uses that to evaporate a lot of water so that his dragout can replenish the water loss as a way of minimizing his effluent as part of his zero-discharge design.

Ted Antonellis

The other big thing is automating the line; he has eliminated cleaners and acids because the panels are never touched by humans. They have no time to build up an oxide. That's taken away almost 60% of the process steps in making a multilayer. I wonder if with increasing automation we can't simplify a lot of our processes if the human is no longer going to be handling the panel.

Antonellis: I would think that would help, right? You always see fingerprints all over cores as they're being handled, or after a process step you see the outline of a fingerprint that maybe didn't get cleaned by the cleaner that was in place. If you take the human contact out, you should be able to eliminate some of these steps.

Cullen: That would be terrific, and we do have some of that technology in place. I have formulated some of our chemistries at higher temperatures specifically to minimize the solution growth. We do that. We do sometimes get pushback from our customers who want to run lower temperatures to reduce power consumption, so we kind of fight that battle. That is a good story; I think maybe a subset of the chemical supply industry needs to really push some of those environmental benefits of smart design of factories.

Holden: Now, it helps that Whelen started out as a greenfield type, but there's a lot to be learned there. One of the most unusual things was the use of this copper ammonium sulfate as a final etchant. That's a big thing, because they use the ammonium sulfate to produce copper sulfate and then turn it to copper oxide and add it back into their pulse plater. They're running a profitable operation there since they etch more copper than they plate.

Cullen: Right, we've done some of the same things. In fact, I have a patent on a process that we had for oxide alternatives, where we would take it back from our fabricators as a service. This was in Taiwan. We had a lot of fabricators in a small area, so we could economically bring the spent material back in, and we would precipitate and purify and then turn it into raw materials for an electroless copper bath. We had other processes even here in Waterbury dating back 30 years, employing some of the same recycling concepts. We would bring the spent baths back in and generate the copper oxide and turn it into other goods. There is still a lot of that going on, but I'm sure there could be more. I mean, even if you look at the recycled circuit board industry, look at all the precious metals that are just thrown into dumps because it's not well thought out. It's not designed in.

Antonellis: But they're doing it internally at Whelen, I believe.

Goldman: Well, I think what has happened in our country is that people already have the processes in place. They already have their discharge permits and everything is set. The costs are already amortized or taken into consideration. It's different when you start out building a new facility; you're going to make it as efficient as possible and try to eliminate the need for permits and such, but I'm guessing the incentive is just not as great for an existing facility.

Antonellis: That's true.

Holden: Part of the incentive is that it lowers your costs, but more so as environmental regulation gets stricter, then it becomes important for survival.

Cullen: But we've seen a couple of these instances. We gotten strict in the United States. People went to China, not just because of environmental, but I'm sure that was a part of it. China is being stricter now, and so we're saying, "Great, we love environmental restriction, because it allows us to deploy processes that are cleaner, and it's a transition, so we can deploy new innovations when there's marketplace needs, like new environmental restrictions." The direct metallization is a prime example. We have this technology, made to anticipate the time when formaldehyde will absolutely be banned, because it would drive a better, cleaner process. It still hasn't happened.

We're seeing it now in China with these restrictions on phosphorous; we have non-phosphorus baths, but what they do is they move to Vietnam. We're seeing something similar right now on one of my PV projects. We had all the technology certified, the value proposition was proven. We're going to build a giant factory for plating solar cells, and the local government said, "Oh, you can't have nickel in that facility." I said, "Well, we have technologies to have zero emissions." They replied, "No, you just can't have it. You can't get a permit to plate nickel."

They moved to a different province, and we're getting that facility designed. What happens? Well, they adopt those rules. So they ended up moving to Thailand, and so there's still Indonesia, Vietnam, Philippines, Thailand, Malaysia. That's where the shops are going instead of just adopting cleaner technology. They move, you know? It's unfortunate.

Goldman: That's very frustrating.

Matties: If you were to give somebody running a wet process department advice, what would be the most important advice that you could give them?

Kologe: I believe, for a lot of fabricators—and that will come from improvement of these advanced manufacturing processes which are still maturing—it will be yields that are going to be the number one thing for this year. I mean, we saw this year with the iPhone, and again, this refers to Asia and mSAP, the new advanced boards that went into the iPhones. The processes and the cost that these companies are paying for them end up being outrageous

I believe, for a lot of fabricators—and that will come from improvement of these advanced manufacturing processes which are still maturing—it will be yields that are going to be the number one thing for this year.

because the current yields are relatively low on these tiny, complex, build-up boards that are going into this generation of cellphones.

Cullen: To turn that into an actionable item for your question, Barry, it would be that so much of our tech service calls come down to "Follow the operating parameters." They tend to share engineers between processes, and I get it; but if they just took the operating conditions to heart, it would save a lot of frustration. Jordan touched on it before. We try to simplify the processes, so you don't need so much instruction. I'm in communications, so I understand that people will read a 30-second email and they won't read a three-minute email, so we try to make the instructions concise. That would be number one.

Matties: It seems like that's where the IOT would have a great benefit—being able to do real time and look and provide operational feedback and make sure they are following the proper steps.

Andy Shaughnessy: Do any of you have any advice to give to circuit board designers and the EEs up front? Anything they should stop doing?

Cullen: Right now, mixed construction is a problem. It's a problem and an opportunity. We have PTFE on exterior layer on both sides and then epoxy in the middle. You know, rigid-flex is always a challenge for material handling and yield.

Kologe: Thermal management is a big problem in high-density circuits utilized in a lot of the automotive designs and mobile. If you get the heat away from the chip, device reliability and performance increase. We really feel that the designers should be open to new ways to mitigate thermal exposure of the chip. They have to think outside the box. There are ways to reduce costs that are out there too.

Cullen: Yeah, these guys are trying all kinds of weird stuff with copper coin, or with thermally conductive film material, and planarization. We do have a copper through-hole fill technology. The adoption of it is a one-time cost with equipment and some process time, but then you end up with solid copper. You can fan those out in layers by increasing dimensions, so you can start with a very fine path out of your chips and then spread it through your circuit board to a much larger dimension. Their conductivity is unrivaled. We're kind of hoping that will head in that direction this year.

Thermal management, of course, is getting very, very important as the voltages of the electric vehicles and just any vehicles are going up. Then, as you said, 50% of the automotive is going to be electronics value. That means a whole lot of circuitry at higher layers, more sophisticated circuitry operating in higher temperature environments, so we've got to do a lot more of the thermal management on the design side.

Shaughnessy: I guess you'd want the designers to work with you guys and with the manufacturing partners as early as possible, but a lot of them don't do that.

Cullen: It can be frustrating because we'll have a meeting with the fabricator, and the fabricator will have a meeting with the designer or with the OEM. Then, we meet with the OEM, and it's he-said-she-said about what happened. We must do a lot more joining up and having smart conversations to connect all those stake-

holders at one time. There is some of that happening. We have some programs, for example, at big Tier One auto suppliers where we get all the stakeholders together and then we come up with a design.

Holden: Don, refresh my memory. The new company that you represent was a combination of what other chemical companies?

Cullen: We have the MacDermid Enthone Industrial Solutions business, so that's the legacy MacDermid, legacy Enthone, and some legacy OMG that was Electrochemicals, and Fidelity. Then MacDermid Enthone Electronics Solutions draws from the same legacy companies for circuit board chemistry as well as the Enthone success in wafer plating and wafer level packaging, redistribution layer and copper pillar, and under bump metallization. We have the Alpha Assembly Solutions which is traditional solders as well as pastes, pre-forms and fluxes, plus some advanced alternative materials and recycling programs. And their Alpha Advanced Materials business, which is materials used to connect the wafer to the substrate, or the substrate to the circuit board, and that's going to be redistribution layer poly and spheres and encapsulants and all that.

There are a couple of other businesses not really in this space. Our Offshore Solutions provides fluids that monitor valves on offshore petroleum production rigs, and our MacDermid Graphics Solutions business does consumables used in the printing industry for transferring images onto printed materials.

So there are select industries like smartphones where they do consume materials from pretty much every one of our businesses. It sounds strange, but it happens. There is much more coordination among our businesses now.

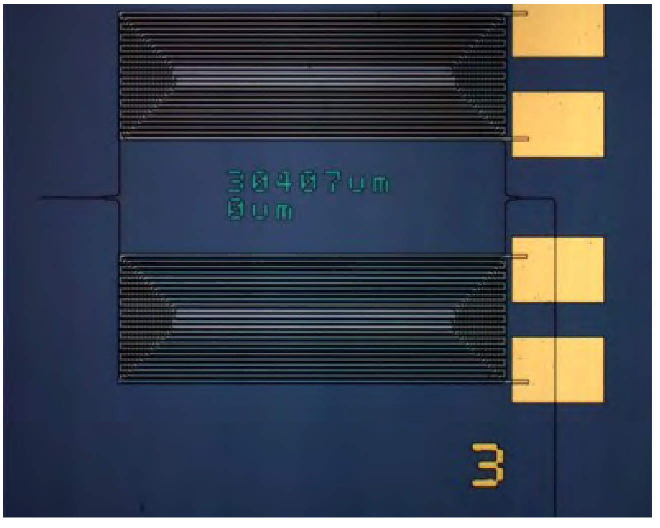
Matties: Is there anything that we haven't talked about that you guys feel we should cover in this conversation?

Cullen: I think those are the primary transitions this year, and each one is going to lead to some growing pains like the HDI into automotive, so we must consider what Happy is talking about with reliability. The substrate-like HDI designs for circuit boards, new designs, so our group who does the wafer metallization, they're talking about a new way of viewing constructions instead of trying to modularize all package designs into fan-out wafer level packaging.

Matties: I see. Thank you very much and take care. We appreciate your time. **PCB007**

Infrared Spectrometer on a Chip

Fourier-transform infrared (FTIR) spectrometers, which are widely used research tools to identify and analyze chemicals, are too large to use in the field. Attempts have been made to develop miniaturized FTIR spectrometers for integration into drones to monitor greenhouse gases, for example, or for integration into smartphones. Scientists at the University of Campinas's Device Research Laboratory (LPD-UNICAMP) in Brazil, collaborating with colleagues at the University of California San Diego in the United States, have overcome these constraints by developing an FTIR spectrometer based on silicon photonics, the technology currently used to produce chips for computers, smartphones and other electronic devices.



Supplier Highlights

Amphenol Invotec Implements AOI Solution from Orbotech ▶

UK PCB manufacturer Amphenol Invotec has implemented Orbotech's Fusion 22XL automated optical inspection (AOI) solution.

Ventec International Group Awarded IPC-4101/40 QPL Certification ▶

IPC's Validation Services Program has awarded Ventec International Group a second IPC-4101 Qualified Products Listing (QPL).

Cirexx Installs Dynachem Cut Sheet Laminator ▶

Cirexx International has installed a Dynachem CSL1700 Cut Sheet Laminator which is capable of handling thin and large panels up to 5 mm (0.2 in.) thick.

Advanced Copper Foil Announces New Arsenic-Free Copper Foils ▶

Advanced Copper Foil and its supply partner, Circuit Foil Luxemburg, are pleased to introduce its new arsenic-free copper foils.

Merlin Circuit Technology Installs New XRF Equipment ▶

Merlin Circuit Technology has announced the purchase and installation of a Fischer XDAL 237 SDD XRF to meet the requirements and ensure compliance to the new IPC 4552A ENIG specification.

Rogers to Show RF/Microwave Materials for Autonomous Vehicles, 5G Apps at IMS2018 ▶

Rogers Corporation will be showing samples of high-performance circuit materials at this year's 2018 IEEE Microwave Theory & Techniques (MTT-S) International Microwave Symposium (IMS).

It's Only Common Sense: Stop Talking and Start Listening ▶

I've been concentrating on listening lately. I mean really listening, not doing what I usually do, which is to wait for the person I'm talking with to finish talking so that I can tell them all the great thoughts I was formulating while they were talking. It's not easy to listen.

Trouble in Your Tank: Pits and Mouse Bites, Part 3 ▶

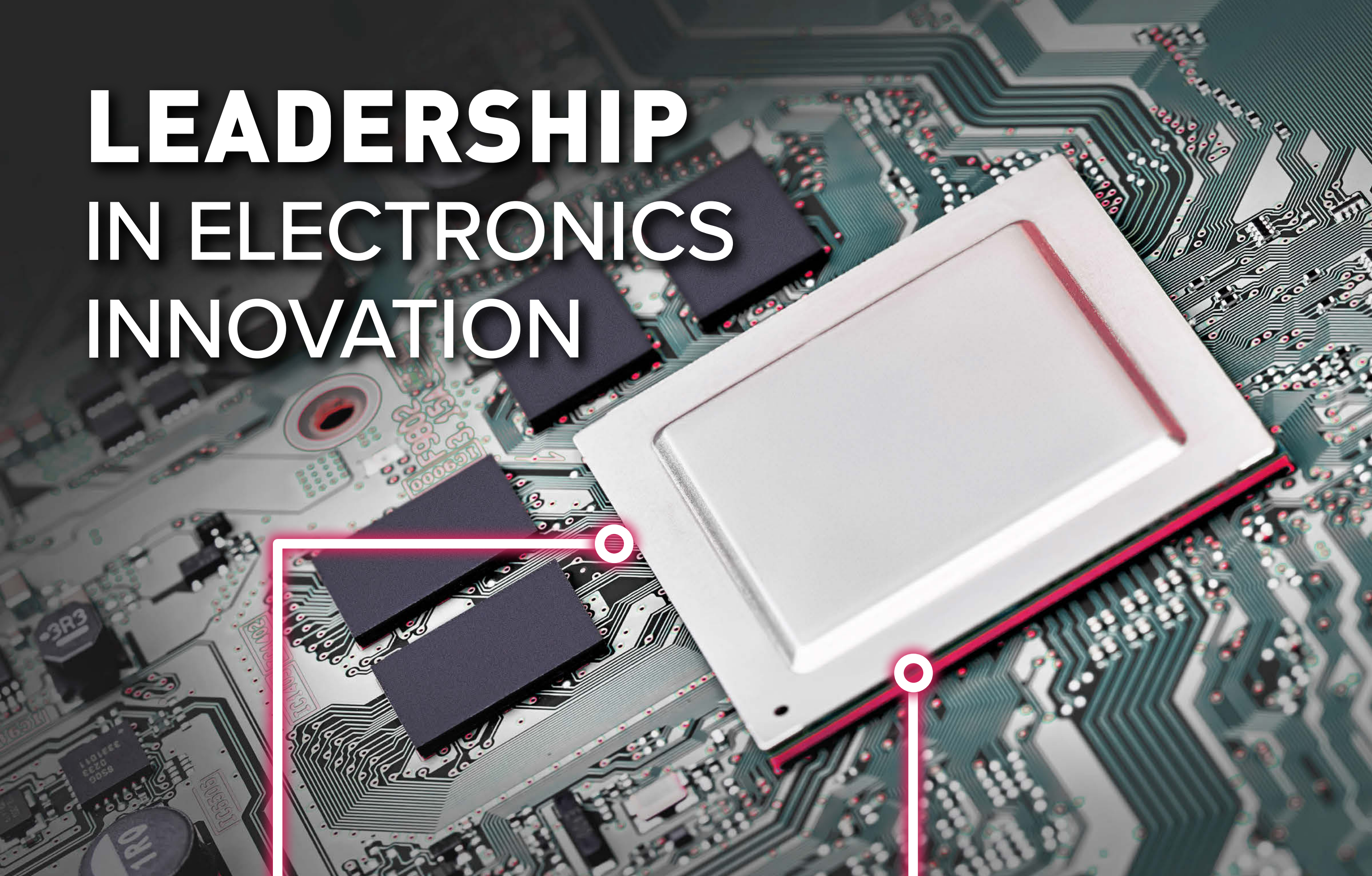
In the first two columns in this series, the author presented two critical areas of the PCB fabrication process thought to contribute to mouse bite and pitting defects seen in production at a fabrication facility.

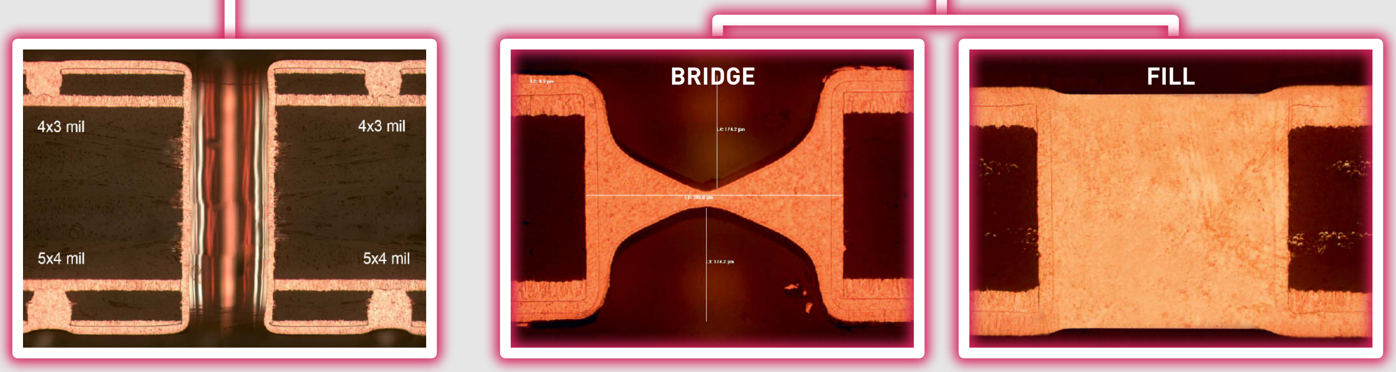
RTW CPCA: Fischer Discusses Automation, Industry 4.0 ▶

Dr. Wolfgang Babel, CEO and president of Helmut Fischer Group, speaks about the latest improvements in their coating thickness test systems to help customers in their automation and Industry 4.0 journey.

Ventec Launches Dk 3.48 Ceramic-Filled Hydrocarbon Thermoset Material ▶

Ventec International Group Co., Ltd. has launched tec-speed 20.0, a ceramic-filled hydrocarbon thermoset material designed for high-frequency applications.





MacuSpec VF-TH 200

Streamlining two processes into a single, easy-to-use system, the **MacuSpec VF-TH 200** is the newest in advanced metallization processing. Achieve through hole metallization and via filling in the same bath, on the same boards, at the same time, in under 60 minutes with minimal copper buildup on panel surfaces.

Systek THF

The future of thermal management in IC packaging is here. **Systek THF** is a two-step bridge and fill process that fills plated through holes with high quality, sturdy, and pure copper metal, allowing for never-before-seen improvements in design miniaturization and heat removal from the package.

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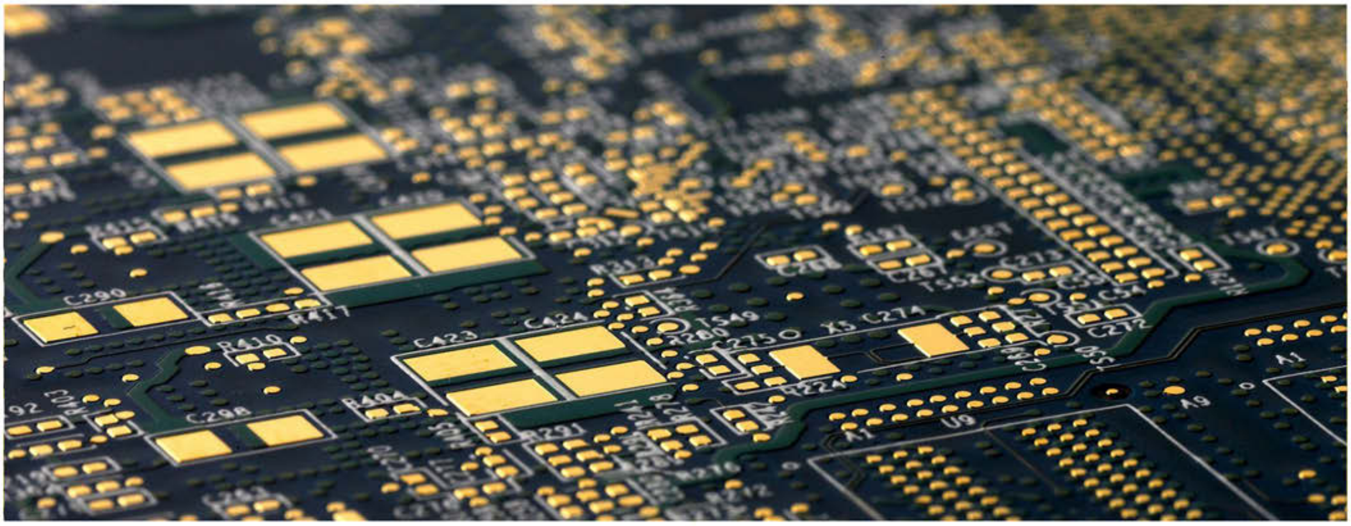


IMAGE SOURCE: ATOTECH.COM

Autocatalytic Gold: How it Fits as a Final Finish

Feature by Rick Nichols
ATOTECH DEUTSCHLAND GMBH

Introduction

Thick gold was originally requested as the solution for making gold wire bonding possible for the electroless nickel/immersion gold (ENIG) process without electroless palladium. This avoided requalification and the risks associated with a new process in a conservative industry. This trend is now being championed by the automotive industry to ensure highest reliability within the gold wire bonding and soldering arena when employing the electroless nickel/electroless palladium/immersion gold (ENEPIG) process.

Thick gold is typically considered to be in the region of 100 nm and, as such, tends to exacerbate some of the issues attributed to the current state-of-the-art immersion gold chemistry at thicknesses of 70 nm. The plating characteristics of the established immersion gold processes are not wholly compatible with thick gold deposit requirements. The reason for the incompatibility is corrosion derived from the long exposure times that are necessary to achieve thick deposits. It must be stressed that thick gold is not always achievable with immersion gold systems. This is especially true if palladium is used as a wire bonding enhancer.

In an immersion process the deposition rate will decrease over time as the deposition layer increases in thickness and density because the availability of electron exchange is reduced. In more extreme cases the source electrons can be limited to relatively small areas of weakness in the underlying deposit and cause exaggerated corrosion events. This can be improved or overcome by employing an autocatalytic type of electroless gold plating system (Figure 1).

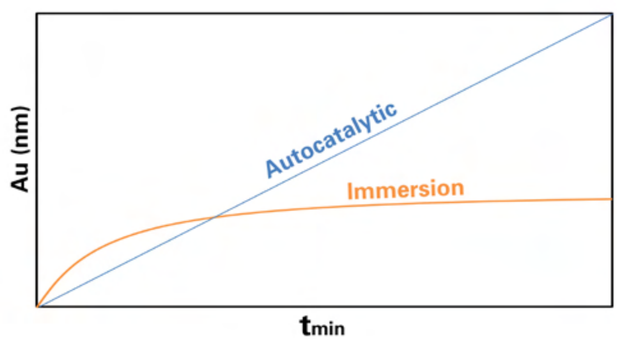
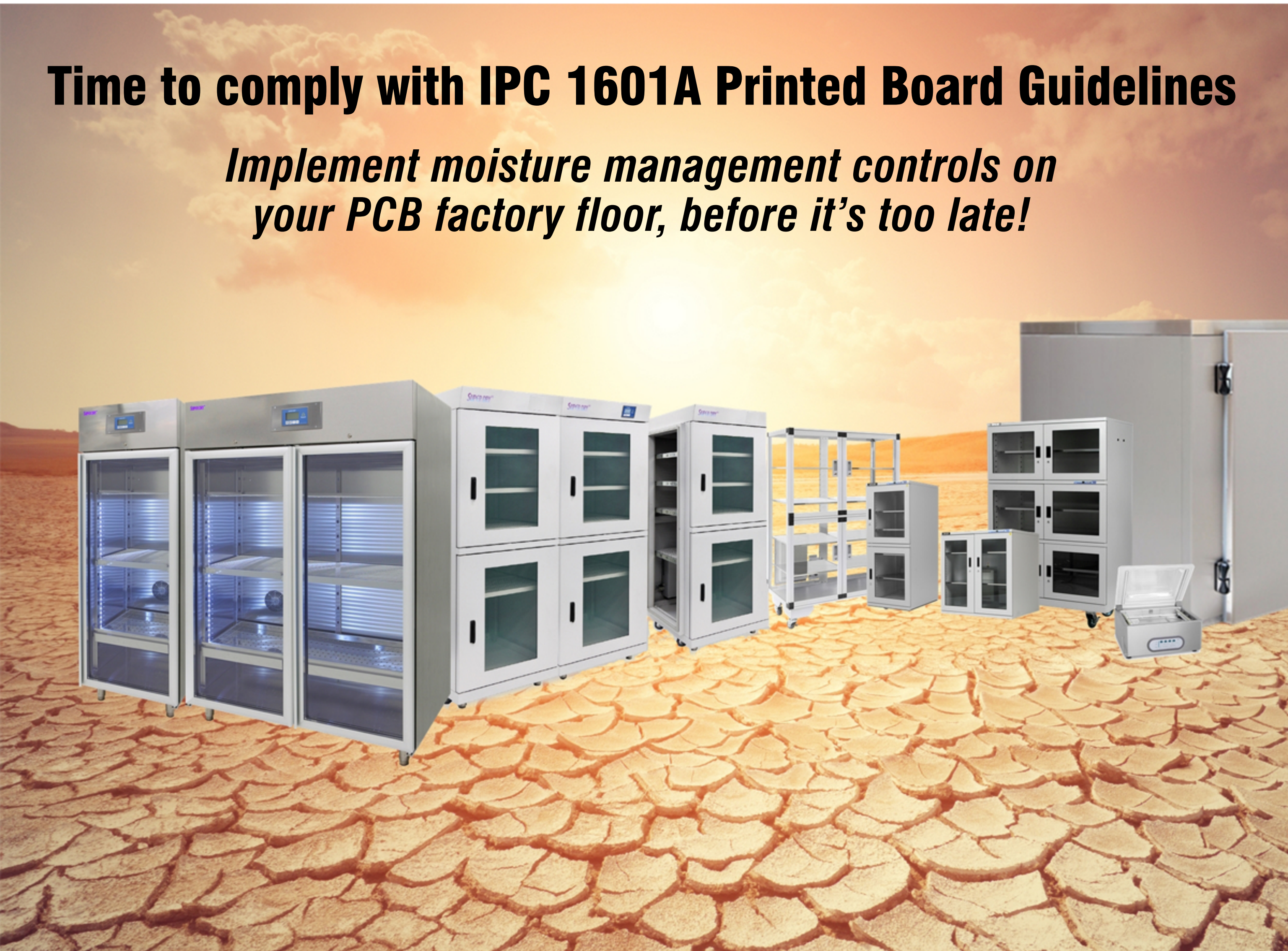


Figure 1: A schematic comparison of the electroless gold deposition rates for immersion and autocatalytic systematic.


Time to comply with IPC 1601A Printed Board Guidelines
Implement moisture management controls on your PCB factory floor, before it's too late!

So far, the systems under discussion have been established systems incorporating nickel as a diffusion barrier. Some more novel universal final finish systems no longer include nickel to achieve more technologically challenging functions. An example is electroless palladium/autocatalytic gold (EPAG). This novel finish was designed with autocatalytic gold as the process of preference. This process is gaining traction by meeting stringent requirements globally.

However, most fabricators would prefer to handle an immersion process to circumnavigate the risks of costly plate-outs that can only be suppressed by continual cyanide dosing and typically higher gold concentrations in the bath. The conundrum is, as ever, performance versus handling—which is usually perceived as cost.

The term 'reduction assisted' is being increasingly cited when referring to immersion gold baths in the electronics industry. The term 'reduction assisted' suggests that the process has autocatalytic characteristics. This type of electroless bath is justifiably regarded as a low-corrosion immersion gold bath as is therefore considered as a potential solution for thick gold plating.

This article will cover the following topics:

- A method to establish the autocatalytic characteristics of electroless gold baths
- An example of the beneficial impact of autocatalytic in a production relevant scenario
- Basic assembly data

Determining the Autocatalytic Properties of an Electroless Gold Bath

Two established electroless gold baths, a reduction-assisted immersion gold bath (RA-Au) and an electroless gold bath designed to be at least partially autocatalytic (SA-Au), were evaluated regarding their respective autocatalytic characteristics.

Platinum-sputtered quartz crystals were used as the working electrodes for a quartz micro balance (QMB). The electrodes were plated as follows:

- Plated with nickel and palladium (SET 1)
- Plated with electrolytic gold only (SET 2)

Both sets of electrodes are required to give a numeric value for the autocatalytic characteristics in %.

SET 1 simulated an ENEPIG finish and therefore immersion process whilst SET 2 ensured that only an autocatalytic reaction was possible. Both sets were plated for 12 minutes in a reduction-assisted immersion gold bath (RA-Au) and a semi-autocatalytic electroless gold bath (SA-Au).

In the case of SET 1, the QMB generated a value that represents the total gold plated and the nickel taken into solution. The nickel taken into solution is an indication for the immersion process. To isolate the gold, a gold stripping process was carried out. The solute was analyzed for gold by ICP-MS (Figure 2).

SET 1 can only verify whether the process is a partial displacement process or 100% autocatalytic. SET 2 coupons can only instigate

Quartz Micro Balance (QMB) determines the mass change Δm_{QMB}

$$\Delta m_{QMB,measured} = m_{Au,autocat} + m_{Au,immersion} - m_{Ni,dissolved}$$

$$m_{ICP,measured} = m_{Au,autocat} + m_{Au,immersion}$$

$$m_{ICP} = \Delta m_{QMB} \ for \ deposition = 100\ \% \ autocatalytic \ part$$

$$m_{ICP} > \Delta m_{QMB} \ for \ deposition < 100\ \% \ autocatalytic \ part$$

Figure 2: A summary of the calculations and interpretation for SET 1.

$$\frac{\Delta m_{QMB}}{m_{ICP\,(Result\ from\ SET1)}} \cdot 100\% = \%\ autocatalytic\ part\ of\ Au\ deposition$$

Figure 3: How SET 2 is used to determine the autocatalytic % of a gold bath.

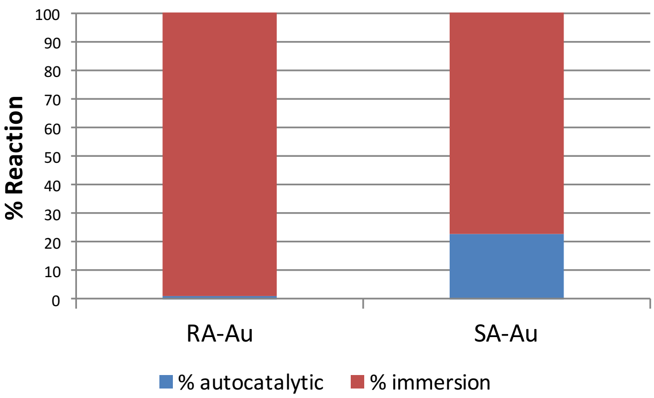


Figure 4: The results according to the evaluation method used.

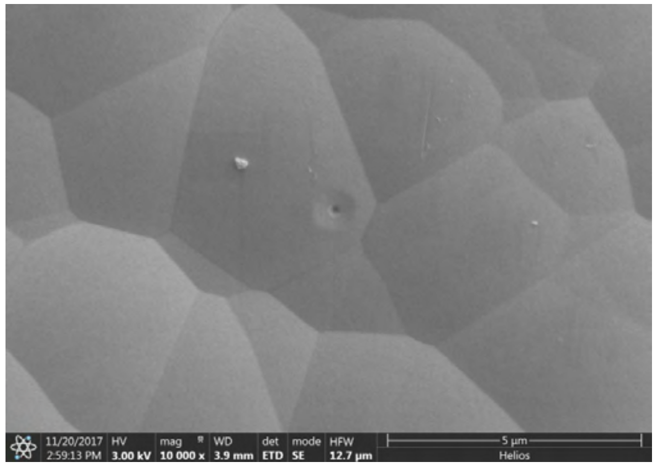


Figure 5: View of pinhole from top surface.

autocatalytic plating, as there are no exchange electrons available. The mass determined by the QMB is then compared to the ICP value from SET1 to determine a value for autocatalytic reaction in % (Figure 3).

The evaluation showed that the reduction-assisted immersion gold does not perform autocatalytically and that the SA-Au is only semi autocatalytic (Figure 4).

An Example of the Benefit of Autocatalytic Electroless Gold Characteristics in Production

Whilst establishing the autocatalytic characteristics of a gold bath is of interest for understanding the mechanism, the results have no meaning unless an analogue impact can be related to production. This section of the article will focus on the issues from fabricators who request thick gold and employ the ENEPIG process.

Multiple final finish layers increase the risk of anomalous failures. Though uncommon, pinholes are a recognized failure mode (the name may vary by region). It is not the aim of this article to establish the root cause of this phenomenon, but to use the failure to showcase the benefit an autocatalytic process. Pinholes are plating failures that increase the potential for corrosion incidents (Figure 5).

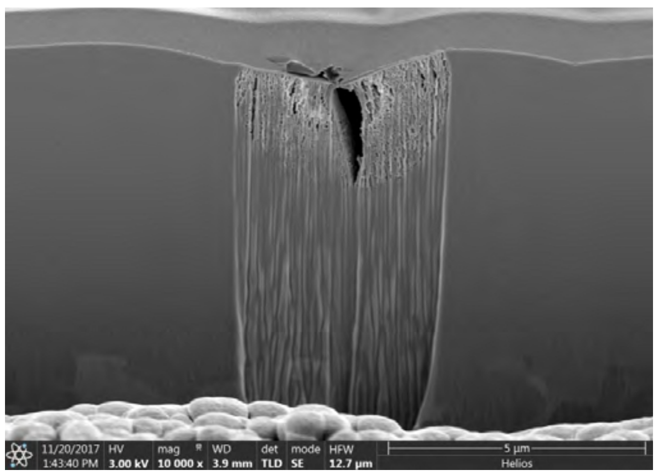


Figure 6: Cross-sectional view of corrosion by the RA-Au.

Reduction-assisted immersion gold is a successful product in the market. However, the immersion process relies on electron exchange mechanism which under some conditions can translate to corrosion. Corrosion refers to excessive localized electron exchange (Figure 6).

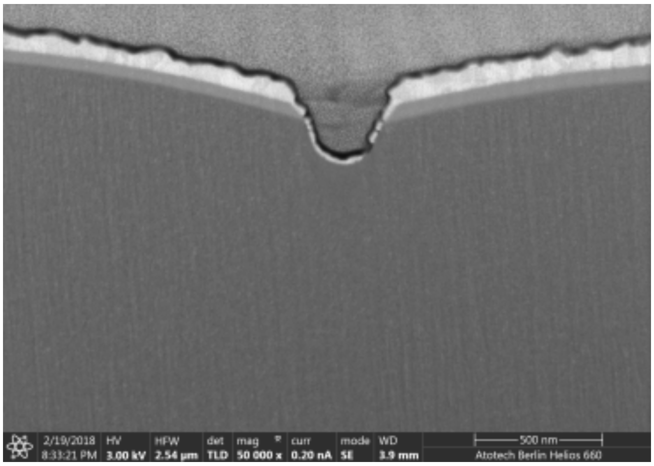


Figure 7: A representation of a pinhole post semi-autocatalytic electroless gold plating.

The plating mechanism and extended plating time required to achieve approximate 100 nm gold thickness cannot satisfy corrosion expectation. Gold plating into the pinhole is a demonstration that the plating process is preferential to the dissolution process in the case of SA-Au (Figure 7).

The SA-Au process has not led to major localized corrosion. The electron has resulted in preferential plating in pinhole rather than nickel dissolution.

Basic Assembly Data

The previous section demonstrated that anomalous defects can be improved by applying an electroless gold with autocatalytic characteristics. However, a cost effective, functional performance is the litmus test for fabricators and OEMs.

Form factor and bandwidth upgrades have rendered soldering as a significant consideration in the electronics assembly field. Good solder joint reliability (SJR) is the prime essential requirement. A recognized simulation tool for BDA/flip chip reliability is high speed shear testing (HSS). The target is to define the quality of a solder joint, specifically in terms of ductility. This is a method to assess resistance to impact.

Figure 8 demonstrates that there is no sta-

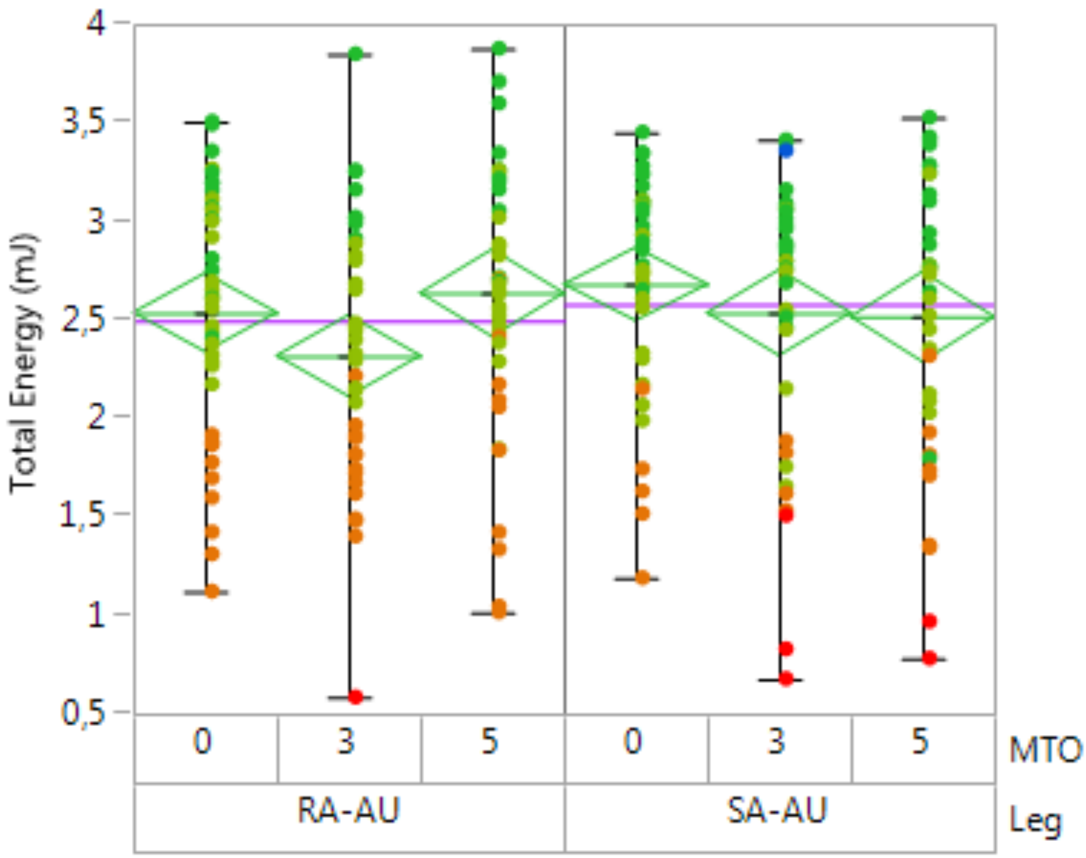


Figure 8: HSS results by lifetime for semi-autocatalytic and reduction-assisted gold baths.

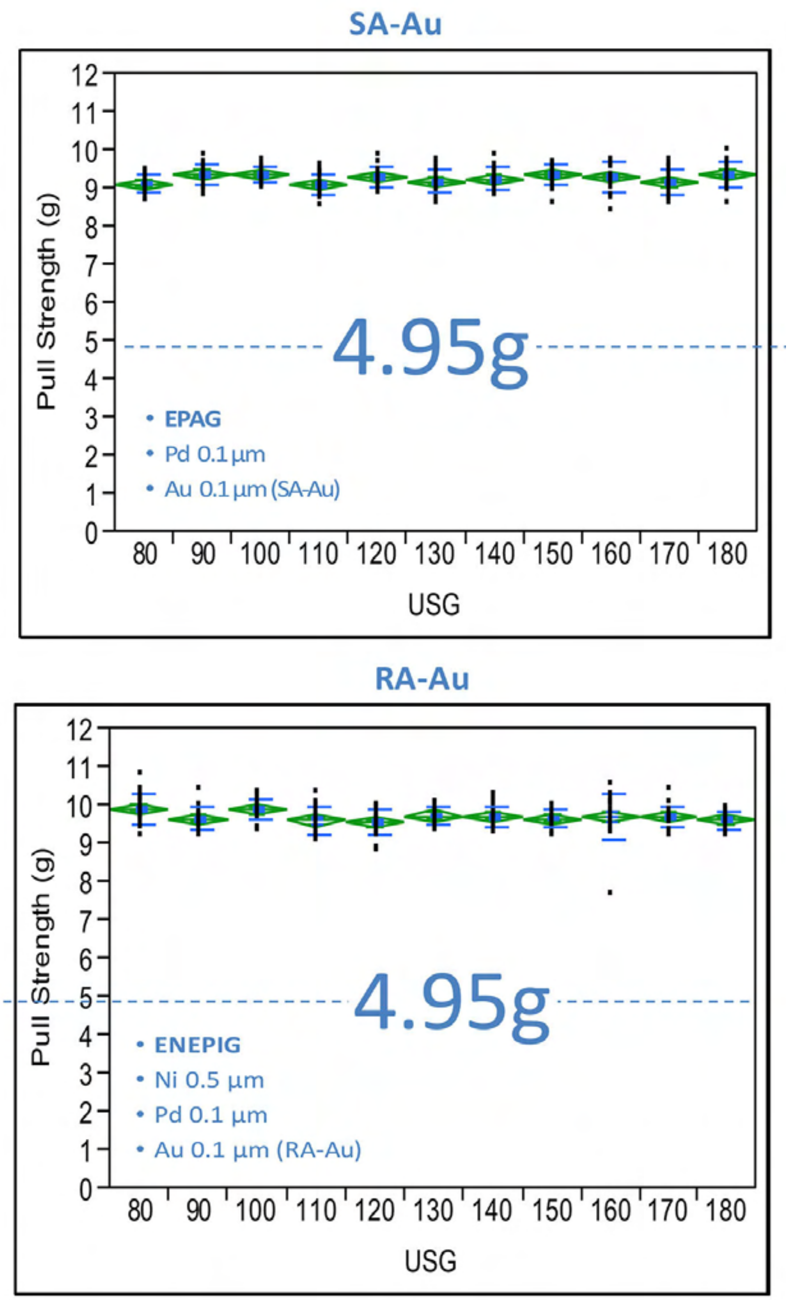


Figure 9: A comparison of the pull strength results for RA-Au and SA-Au after ageing at 150°C for four hours.

tistical difference between the performance of the electroless gold bath that has autocatalytic characteristics (SA-Au) and the reduction-assisted immersion gold bath (RA-Au). This observation is true independently of bath age and represented by MTOs.

As previously mentioned, novel high-performance finishes do not include nickel as a diffusion barrier and employ autocatalytic electroless golds as a state-of-the-art solution. An example is electroless palladium/autocatalytic gold (EPAG).

To evaluate gold wire bonding performance, EPAG, employing a semi-autocatalytic electroless gold, was compared to an ENEPIG finish, employing a reduction-assisted immersion gold. In both cases 23 µm Tanaka gold wire with a breaking strain of 9.9 g was used. To maintain a level playing field the wire bondable gold finishes were plated at 100nm. The evaluation method was cold ball pull testing (CBP).

Figure 9 demonstrates that both gold finishes achieved the required pull strength of 4.95 g which is 50% of the breaking strain of the wire used for the test. This satisfies the pass criteria according to DVS 2811.

Conclusion

Existing electroless gold baths with autocatalytic characteristics are a drop-in solution to replace immersion gold baths in ENIG, ENEPIG, whilst being state of the art for the EPAG process. It has been demonstrated that a gold final finish with autocatalytic characteristics has no performance drawbacks but can be shown to have the benefit of reducing or eliminating corrosion when higher gold thicknesses are required. It has also been shown that reduction-assisted immersion golds do behave autocatalytically.

For process sequences or more information regarding semi-autocatalytic gold baths or the latest in the development of a fully autocatalytic gold bath that can eliminate corrosion at thickness of >100 nm please contact the author. **PCB007**

Rick Nichols is global product manager, surface finishing, with Atotech Deutschland GmbH.

IPC E-TEXTILES 2018

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Email ChrisJorgensen@ipc.org for availability.

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Electronics Industry News and Market Highlights

Global Flex PCB Market: Growth Through 2026 ▶

The opportunity in this market is expanding at a healthy CAGR of 11.80% between 2018 and 2026, increasing from $13.51 billion in 2017 and rising to $38.27 billion by the end of 2026.

Can a Home WiFi Router Act as a Medical Sensing Device? ▶

New research that could transform the future of healthcare will investigate whether it is possible to reuse WiFi radio waves as a medical radar system.

Researchers to Develop Self-Evaluating Robots ▶

Robots can do a lot of things—assemble cars, search for bombs, cook a meal or assist in surgery. But something they can't do is tell you how they are doing.

Novel Fibre Optic Receiver Helps Researchers Break Data Transmission Record ▶

Optical connectivity requirements imposed by such the data explosion of 5G and IoT means there's a growing need for energy-efficient, multi-channel links with fast data transfer rates.

Smart Technology, New Business Models, and Cross-industry Digitization Revolutionize the Energy & Power Industry in Asia-Pacific ▶

A rise in battery energy storage capabilities, emerging start-ups, and an increase in merger and acquisitions drive expanding growth opportunities.

Six Predictions that Will Shape the Global Energy Storage Sector in 2018 ▶

Frost & Sullivan's recent analysis finds that the total installed capacity will grow 15.9% between 2017 and 2018, and the top six countries will complete installation of 1,369 MW of grid-scale ESS projects in 2018.

Flexible Fingerprint Sensors Promise Embedded Secure Access ▶

Researchers from Holst Centre have demonstrated a new class of flexible, large-area sensor technology for detecting finger and palm prints.

Global Semiconductor Sales Up 20% Year-to-Year in Q1 ▶

The Semiconductor Industry Association (SIA), announced worldwide sales of semiconductors reached $111.1 billion during 2018Q1, an increase of 20% compared to 2017Q1, but 2.5% less than 2017Q4.

Telecommunications Companies Modernize, Diversify in Face of Competition ▶

Telecommunications companies are under threat from over-the-top (OTT) services that enable consumers to communicate over the internet via streaming content and apps such as Skype, WhatsApp and Viber.

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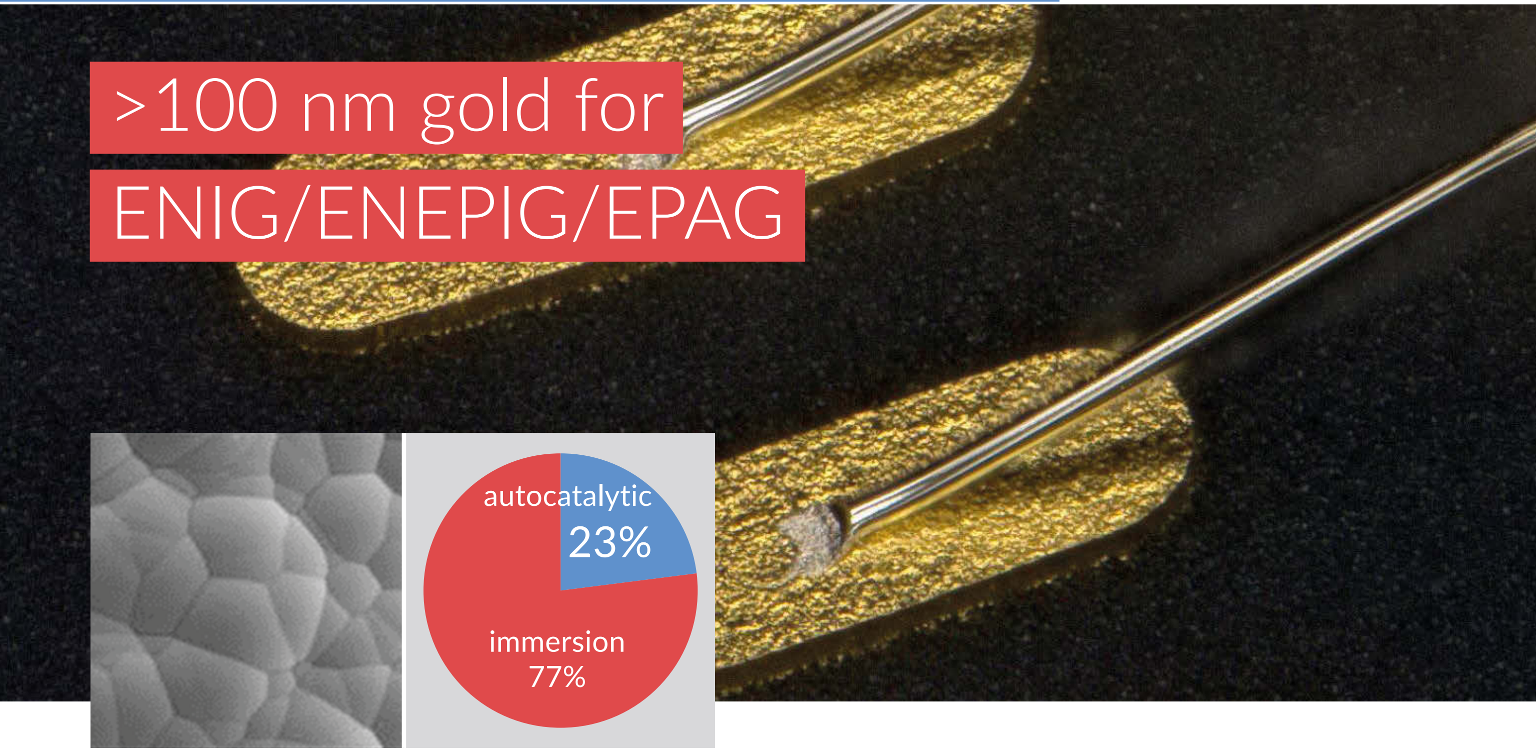
The factors driving this market are the continuous growth in the use of on-board magnetic sensors for consumer electronics applications and the role of on-board magnetic sensors in navigation.

Aurotech G-Bond

Corrosion free thick electroless gold

ATOTECH

>100 nm gold for ENIG/ENEPIG/EPAG



Topography of the Nickel after gold stripping: Ni µm/Pd 0.1µm/Au 0.1µm

No excessive nickel at pin hole even at 100nm gold plating

Aurotech G-Bond provides an ideal corrosion free for ENIG, ENEPIG and high capability, nickel free EPAG finishes at a deposition of >100nm.

Aurotech G-Bond is an alternative to electrolytic gold. The thickness can be manipulated to ensure best wire bonding results. Plus no more yield decreasing bussing structures have to be designed into the process.

The superior performance of Aurotech G-Bond is based on a gold concentration of 0.8 in the bath which is 50 % less than the marketed alternatives.

Reliable bonding with next generation wires such as silver is also possible. (Data taken from EPAG).

0.8 g/l

gold: ensures economic benefits

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Developments in Wet Processing: Beyond Spraying and Dipping

Ladle on Manufacturing
Feature Column by Marc Ladle, VIKING

Spraying and dipping! Wet processing is based on two simple principles: Spray the work piece or immerse it in a bath. Most of the things you do in a complex machine you could also do with a series of buckets, but the results are likely to be much less reliable or efficient.

My work in the printed circuit industry has involved roles in many factories and using a wide variety of equipment, both new and old. At times, the major battle was just to keep the conveyors turning for another day. Enhancing the process effect was often a matter of slowing down the process to give a little more time for things to happen. Right now, I am involved with the supply of a variety of equipment, some of which I would regard as pretty standard and others that involve new ideas that have the potential to solve particular problems.

The target for equipment sellers is to be able to offer a machine that has advantages over the competition. This drives development, but it is still sometimes difficult to let the end users know what is new on the market.

Some of the following examples may be reasonably well known and understood but they show how the equipment can be tailored towards a purpose even though the working basis of the machine is standard.

Earlier this year I was involved in installing an immersion tin line for a customer. The process and the chemistry are not new or special in any way. However, the machine was built to overcome a problem with the immersion tin chemistry, which makes the process more labour intensive to maintain. Immersion tin chemistry does not like to be agitated very much. Bubbles in the solution cause solids to form, which degrades the solution and causes problems with the hardware. The solids settle to the bottom and can damage pumps and heaters, or at the very least make them less effective. The machine I was working on was a horizontal process, which means the immersion tin chemistry is applied in a flood rinse. This effectively means that the conveyor is flooded with chemistry, so the panel is in a complete bath while it is passing through that section of the line.

The idea that is relatively new is to remove the traditional pumps from the sump and replace them with low impact and low-pressure

impellers, which move the solution in a very gentle way. The traditional pump is like an outboard motor on a boat—it is very effective at moving liquid, but it also causes quite a lot of froth and disturbance. In comparison, the revised design is more like a paddle. In the right hands it can create a gentle liquid movement with hardly a stir being seen on the surface. This gentle movement is ideal for immersion tin and this process development has the potential to reduce downtime, increase chemical life, and even improve the rate of deposition.

This machine is also the first time I have used remote water heating to control the temperature of the working solutions. Again, the advantage of this process is that the surface temperature at the heater can be much more carefully controlled so there is less heat shock which can also damage the chemistry. I can only say I was impressed with this and the accuracy of control was good. It is something I would recommend to enhance the control and effect of the heating if there is room in the factory to accommodate it. The working temperature of the water heating system does not need to be much higher than the highest temperature for the heated solutions. In most cases, 10 degrees difference should be more than enough so there do not have to be super-heated pipes running around the factory.

Figure 1: Horizontal immersion tin process. All chemical tin solution movement is driven by low impact propeller pumps.

The initial tests of the process are very positive and from what I can see it offers a real step forwards in a process that has remained relatively unchanged for a long time.

When you are dealing with processes which may have been established for a number of years, it is not always obvious how to adapt them to suit current product needs and requirements. Hole sizes get smaller, blind holes are more prevalent, and aspect ratios are increasing, all of which make it tough to get a good effect of chemistry both on the surface and inside the hole. Often, these two requirements conflict with one another.

Most fabricators don't have the luxury of updating equipment as often as their customers update their product designs. This makes it critical that when you do replace equipment, it has the right set of process enhancements to fit your predicted plans for the next few years. For this reason, it is important to get a good understanding of what is possible. There is no substitute for a regular and deep study of the market just to keep an eye on what is going on with a view to understanding how it could be applied to your own processes and machinery.

A few years back, a customer asked me to include a high-pressure rinse as part of a dry-film pre-clean line. The requirement seemed a little unusual to me but since he had asked, I investigated what we could offer. It became obvious that spray pressure was not a problem; we could offer various formats of pump and spray systems that could run at a pressure of over 150 Bar. The problem is that it is easy to damage material when you use this type of high-pressure system. We did some experiments and it seemed the best effect for his purpose (to remove particles stuck to the walls of drilled holes in certain exotic materials) was an 80 Bar pump and spray system. This was another example of a successful process development to overcome a process need. The high-pressure system can be switched off when processing thin and delicate materials to ensure they are not damaged.

More commonly, we apply ultrasonics to processes to enhance the cleaning of surfaces and the cleaning and wetting of holes. Often it would be possible to run the same process without ultrasonic drivers being included but the failure rate is likely to be higher. Everyone would like to have a zero-failure rate, and this is one way to get closer to it. To apply the ultrasonic system, immerse the process panel while it is passing the driver system, so it can't be used with a spray process but in most cases, it is usually possible to combine a mixture of flood and spray application to get the best effect. Different frequencies can be applied to give the most effective result depending on what you are trying to remove.

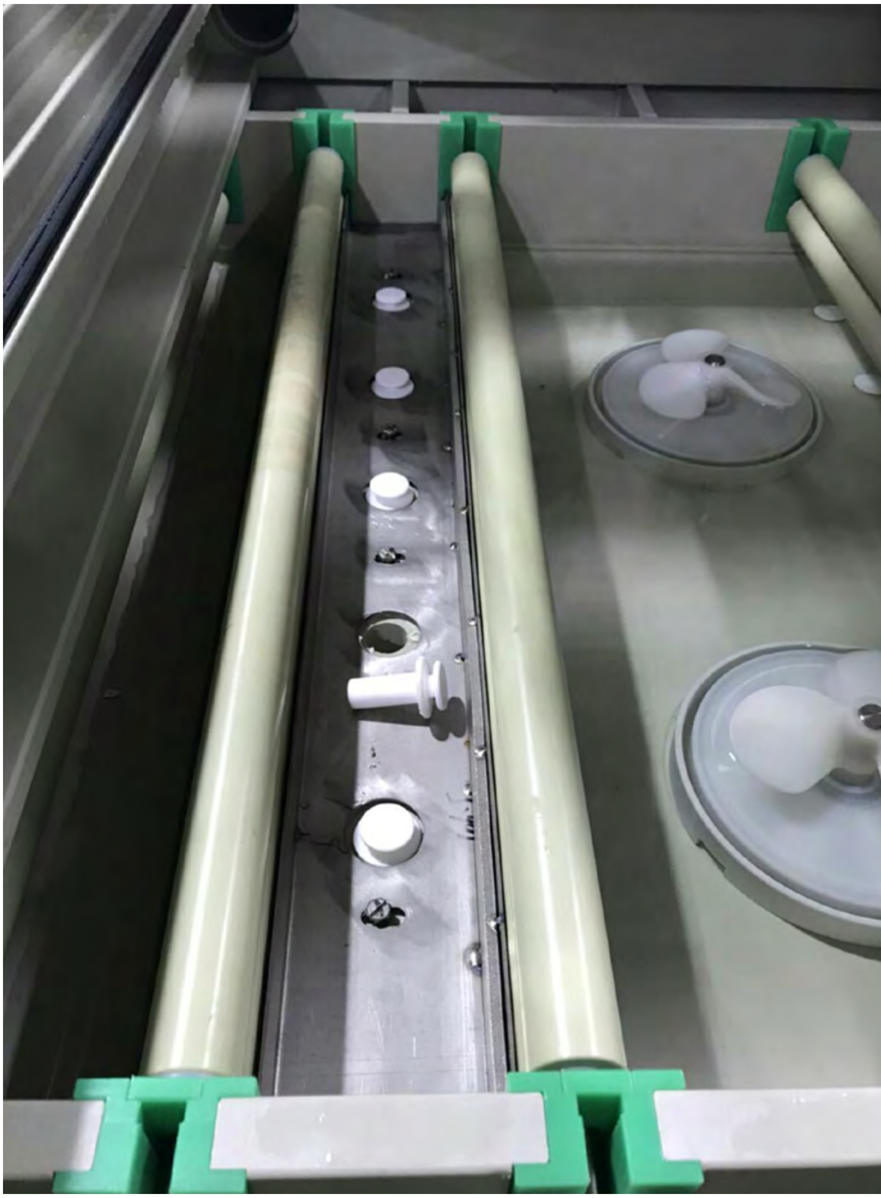


Figure 2: Fluid movement inside the immersion tin chamber is driven by gentle propellers to minimise bubbles in the solution. This reduces maintenance and extends solution life.

The best effect is gained if the machine is designed for these types of features right from the start. In some cases, it may be possible to add features like ultrasonics to an existing line, but the effect is less likely to be perfect. Machines are usually designed to be as small as possible, so adding extra hardware is usually a compromise and splitting a line to add an extra module in the middle is quite a tough job.

Some parts of the manufacturing process require the most even chemical effect possible across the working panel. Electroplating and etching are prime examples.

For several years, people have been using reverse-pulse rectification to enhance the plating effect and to enable them to achieve higher aspect ratios of panel thickness to hole size with less variation of plating-hole thickness. Reverse pulse uses a high-current, short-period reversal of polarity to unplate material from the product surface. The high current means that the effect is greatest where the material is depositing most thickly during the forward current cycle. This gives a smoothing effect and a more

The high current means that the effect is greatest where the material is depositing most thickly during the forward current cycle.

even thickness both on the surface and in the holes. Right now, the effect can be further enhanced by using continuous plating methods that move the panel though the plating cell on a conveyor system so the whole panel has the same view of the anodes. This enhances the distribution on the surface and in the holes, which can allow you to go much further with the products you are able to run. Downsides to the process include a larger footprint in the factory than the equivalent conventional plating process, but clever layout can often gain some of this space back.

For etching, the vacuum process has really started to move things on. It has always been tough to achieve exactly the same effect on the top and bottom sides of the working panel as it passes though the etch machine. A lot of the reason for this is simply gravity. The bottom-side spray hits the panel and the drops back off assisted by gravity, which leaves a space for the next spray to hit the panel. On the top side the spray hits the panel and stays there. This means solution turnover is much less effective on the top side because of the puddle which remains. To make matters worse the puddle runs off the edges of the panel but the closer to the centre you get the harder it becomes to move the solution.

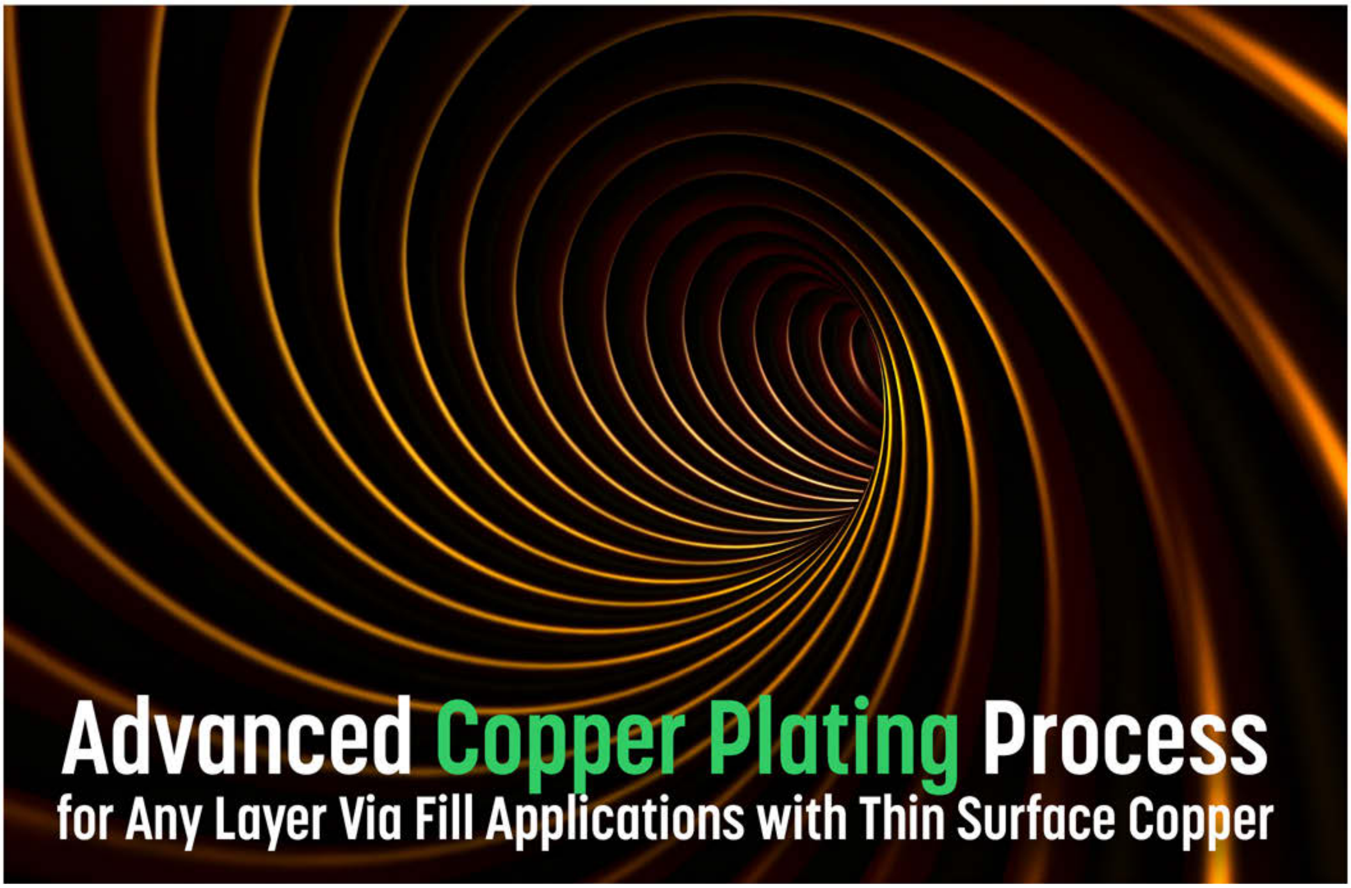
Vacuum etch uses a vacuum head following every spray bar. This removes the puddle of solution, which allows the subsequent spray to be much more effective. Solution turnover at the surface is much improved and results in the top and bottom sides being more evenly etched than with the traditional process. As process requirements become more extreme, with thicker metal layers being etched, the vacuum gives more and more of an advantage.

A further enhancement to the etched result is possible by having an atomising etch chamber after the main etch chamber. This allows you to target the foot of the etched metal feature to achieve a squarer cross-sectional profile. This approach is not widely used but it certainly offers a further improvement for the most testing of product designs.

We are always trying to find ways to offer a more efficient, faster, smaller, more accurate process. To be able to best apply that to a particular factory it is important to understand what needs to be achieved. Wet process equipment is usually expected to last at least 10 years, so getting a handle on the roadmap for process development is imperative to ensure a new machine is fully up to the task. Ideally, suppliers work together with their customers to discuss the pros and cons of the types of features detailed in the examples above.

Currently, the company I work for is busy, which means the industry we supply is busy and process development along with investment in new equipment is strong. This is a good sign for the future of electronic manufacturing; long may we continue to find new ways to enhance the effect of spraying and dipping your panels. **PCB007**

Marc Ladle is director at Viking. To contact Ladle or to read past columns, click here.



Advanced Copper Plating Process
for Any Layer Via Fill Applications with Thin Surface Copper

Feature by Saminda Dharmarathna, Christian Rietmann, William Bowerman, Kesheng Feng and Jim Watkowski
MACDERMID ENTHONE ELECTRONICS SOLUTIONS

Abstract

Copper-filled microvias are a key technology in high-density interconnect (HDI) designs that have enabled increasing miniaturization and densification of printed circuit boards for the next generation of electronic products. Compared with standard plated through holes (PTHs), copper-filled vias provide greater design flexibility, improved signal performance, and can potentially help reduce layer count, thus reducing cost. Considering these advantages, there are strong incentives to optimize the via filling process.

This article presents an innovative DC acid copper via fill formulation, for vertical continuous plating (VCP) applications which rapidly fills vias while minimizing surface plating. For instance, a 125 µm x 75 µm via was filled with just 10 µm copper deposited on the outer layer surfaces. X-ray diffraction studies were done to obtain information about the grain structure (texture) of the deposit. Based on determination of the Lotgering factor, the study shows that the (111) plane has a slight preference (Lotgering factor ~0.2) over other typical planes (e.g., 200, 220, and 311). X-ray diffraction (XRD), focus ion beam (FIB), and scanning electron microscopy (SEM) data show that there is no significant change in the grain structure even after the bath was aged up to 150 Ah/L. This formulation contains no harmful formaldehyde, which was classified in 2016 by the European Union as a carcinogen, thereby restricting its use in electroplating formulations. These regulations in the future, could expand into other regions as well. Therefore, having no formaldehyde is an added advantage for safe operation and waste disposal.

Introduction

The PCB industry has evolved immensely over the last few decades in response to the need for increased densification and miniatur-

ization of designs. The use of blind and buried vias, made possible in part by advances in plating chemistries, have enabled the use of sequential build up (SBU) technologies to accommodate more and finer pitch surface mount components[1]. These new designs with blind and buried vias directly impact multilayer processing. Reliable via filling materials and methods are necessary and in high demand to fulfill the needs of PCB boards with deeper blind and buried vias.

Acid Copper Via Fill

Electrodeposited copper has become the fundamental choice for via fill applications due to the exceptional conductivity and cost. Electroplating is done in a typical electrolyte consisting of acid, copper and chloride ions. Sulfate-based electrolyte systems are preferred in the PCB industry owing to their low cost, convenient operation, safety and ease of waste treatment[2]. Compositions for copper via filling baths typically run with high concentrations of copper (up to 250 g/L copper sulfate) and lower concentrations of acid (approximately 100 g/L sulfuric acid). An additive-free electrolyte will give a deposit with poor physical properties and conformal plating. To get the desired consistent via fill while plating a minimum amount of copper on the surface, carefully designed additives are vital. These additives are key for filling vias of various diameters and depths. Typical systems will contain carriers, brighteners, and levelers. In theory, it is possible to fill vias with only carrier and brightener[3]. However, from a practical standpoint, the dimple will be large, and fill will be conformal, also the brightener concentration will be very low making it difficult for the cyclic voltametric stripping (CVS) analysis[4]. To raise the concentration of the brightener and obtain a good fill, levelling agents must be used.

Carrier and leveler in these formulations act as suppressors in different ways and can be classified as different types of suppressors[5]. Type I suppressors, like carriers, can be deactivated by the brightener (antagonistic, selective adsorption to chloride only) whereas type II suppressors, like levelers, do not undergo deactivation (synergistic, non-selective adsorption due to electrostatic interaction).

Carriers or suppressors are typically high molecular weight polyoxyalkyl type compounds. Typically, carriers are adsorbed at the surface of the cathode where they form a thin layer by interacting with chloride ions. Thus, carrier suppresses the plating rate by increasing the effective thickness of the diffusion layer[6]. Consequently, the energy level over the cathode surface topography is being equalized (same number of electrons locally for plating at any cathode surface spot) so that the resultant deposit becomes more uniform and a more evenly distributed copper deposit thickness can be obtained. On the other hand, brighteners increase the plating rate by reducing the suppression. They are typically low molecular weight sulfur-containing compounds, also called grain refiners.

Levelers typically consist of nitrogen-bearing linear/branched polymers, heterocyclic or non-heterocyclic aromatic compounds being typically quaternized (positively charged). These compounds will adsorb selectively on high current density sites such as edges and corners, local protrusions and prevent copper over-plating in high current density areas[7].

Via Fill Mechanism

The difference in growth rate of copper inside and outside any via is governed by the additives. Figure 1 shows a schematic representation of via growth. Chemical adsorption is exaggerated here to show the different role played by each additive. However, both selective and non-selective adsorption occur during plating. Additive compositions must be controlled in a set range to get the desired “bottom-up filling.” Analytical tools such as CVS analysis, the most common in the industry, may be utilized, although other techniques such as HPLC (high performance liquid chromatography) are available to determine the concentrations of the additives.

In Figure 1, wetter or suppressor is represented with green, leveler with red and brightener with yellow. Wetter molecules predominantly adsorbed on the surface suppressing

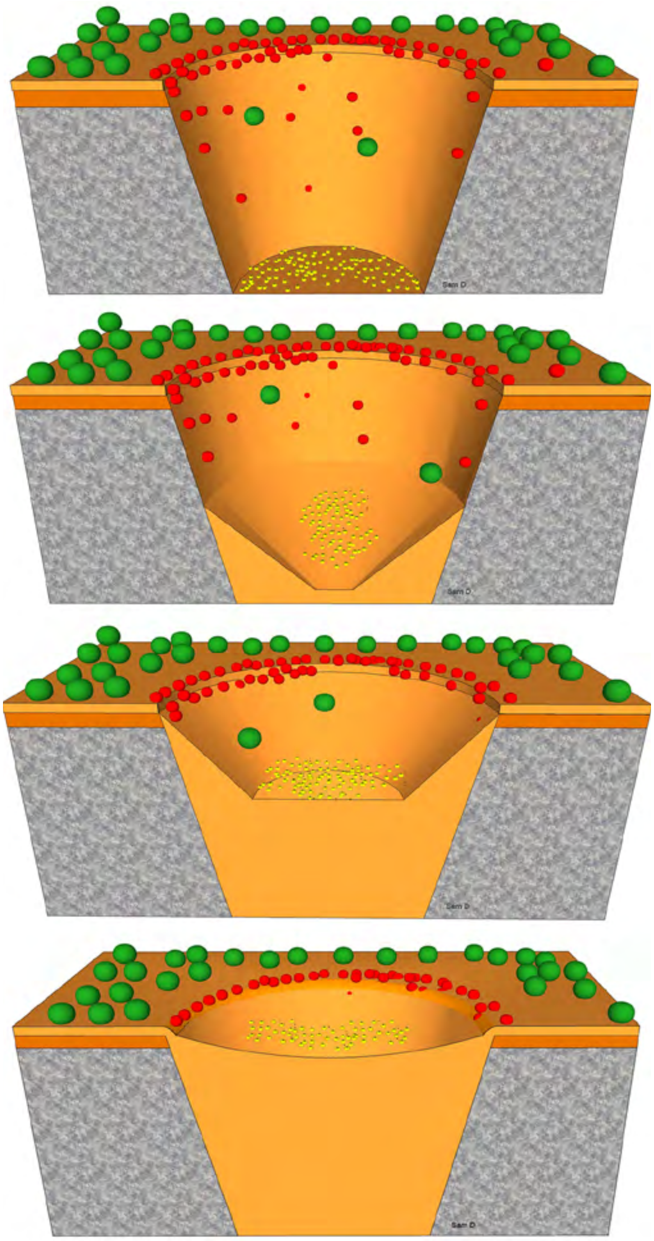


Figure 1: Schematic representation of bottom-up filling.

the surface, while the leveler molecules adsorb selectively on to the high current density areas due to the positively charged, quaternized N group. This prevents over-plating at the edges and avoids premature closure of the via leaving voids in the center of the via. Brightener, being a small sulfur-containing molecule, diffuses faster into the via and accelerates the plating[8]. Since the geometry of the via changes during the plating process, the brightener becomes concentrated inside the via causing a rapid plating in the via. This is called the curvature-enhanced-accelerator coverage (CEAC) mechanism[9]. Finally, when the via gets leveled with the surface and the plating rates inside the via and on the surface become equal, the bottom-up filling stops.

Parameter	Range	Optimum
Current Density	1.0–3.5 ASD (10–32 ASF)	2.2 ASD (20 ASF)
Temperature	20 –27°C (8–80°F)	23°C (73ºF)
Wetter	9–25 mL/L	10 mL/L
Brightener	0.5–1.5 mL/L	1 mL/L
Leveler	0.5–2.5 mL/L	1.5 mL/L
Copper Sulfate ($CuSO_4$.**5** H_2O)	230–250 g/L	240 g/L
Free Sulfuric Acid 66° Be Electronic Grade	55–65 g/L	60g/L
Chloride Ion (Cl^-)	40–60 ppm	50 ppm

Table 1: Bath components and plating conditions.

Conditions and Bath Components

Table 1 shows the operational conditions and optimum additive levels. Typically, via fill baths have high copper and low acid to achieve the desired bottom up fill.

Test Vehicles

Test panels with different via sizes were used during the evaluation. The thickness of the test vehicles used in the process evaluation were 1.6 mm with via diameter range from 75–175 µm, and the via depths of 75 µm and 100 µm. All geometries for each test board thickness were plated at the same time in the same tank and later the fill ratio was calculated by using cross-section analysis. Fill ratio is defined as:

$$Fill\ Ratio = \frac{B}{A}\ X\ 100\ \% \qquad \text{Eq. 1}$$

Figure 2 shows a typical cross-section of a filled via with a dimple; dimple is the fill difference A-B.

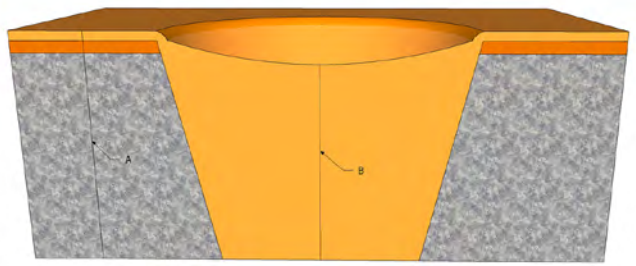


Figure 2: Via fill ratio.

Cross-Section Analysis

Cross section analysis was started with the sample preparation process by punching or routing sections from a desired area on the board or test panel. Pre-grinding of the coupon was done to get a flat surface closer to the through holes. Plastic index pins were used to align the coupon vertically to the grinding surface. A fast-cure acrylic resin was used to mount the coupons. A ratio of 1-to-1, hardener-to-resin, was used to provide optimum penetration and a quick cure rate (10–15 minutes). After the section hardened they were subjected to grinding, polishing, and microscopic inspection. Figure 2 shows a cross-section of a via indicating the points of measurements.

Process Flow

The process flow included the following operations:

- Acid cleaner: wets the hole and remove any organic contaminants
- DI water rinse
- Micro-etch: further smooths the surface and ensures excellent copper to copper adhesion
- DI water rinse
- Acid dip: acidifies copper surface prior to plating
- Electroplating of copper in acid copper bath

Results and Discussion

Via Fill and Bath Plating Performance

Initial plating results showed that excellent filling can be obtained with different surface copper amounts. A 125 x 75 µm via can be filled even with only 10 µm copper on the surface as shown in Figure 3. Flow rate variation showed that the formulation has a wide range of operation from 0.4 LPM to 0.8 LPM with results shown in Figure 4. A larger dimple was

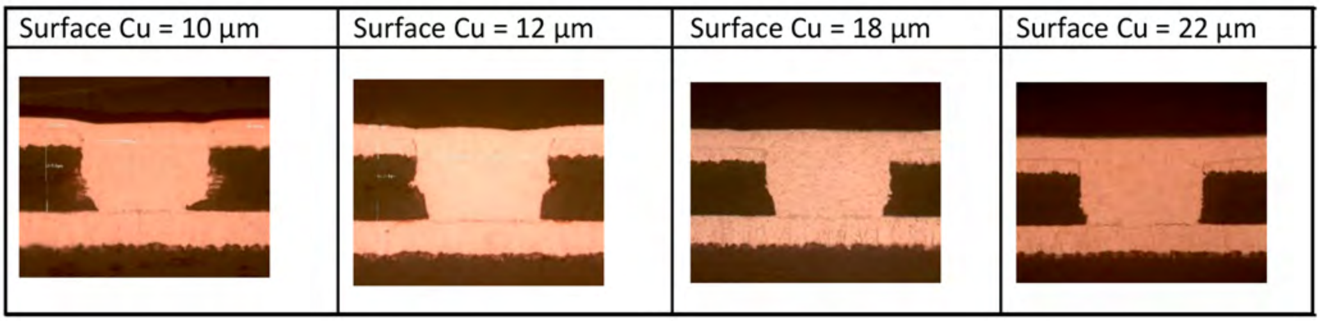


Figure 3: Via fill performance of 125 x 75 µm with different surface copper.

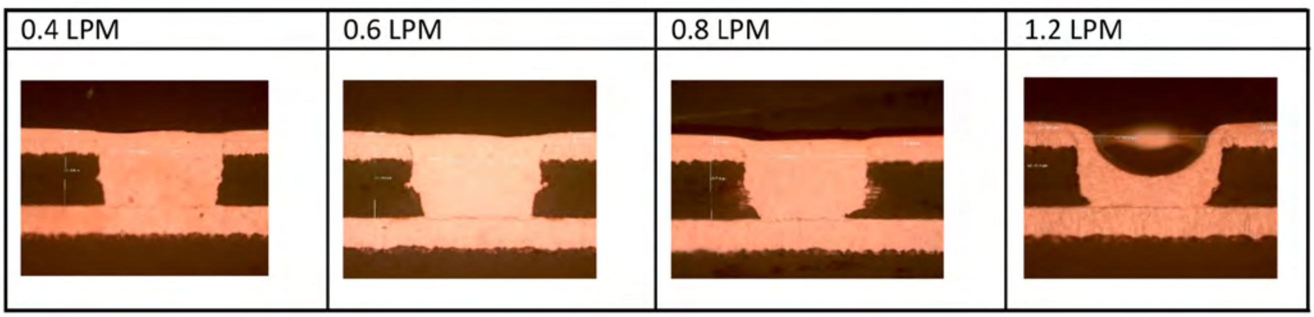


Figure 4: Via fill performance of 125 x 75 µm with different solution flow rates of 0.4, 0.6, 0.8, 1.2 liters per minute (LPM).

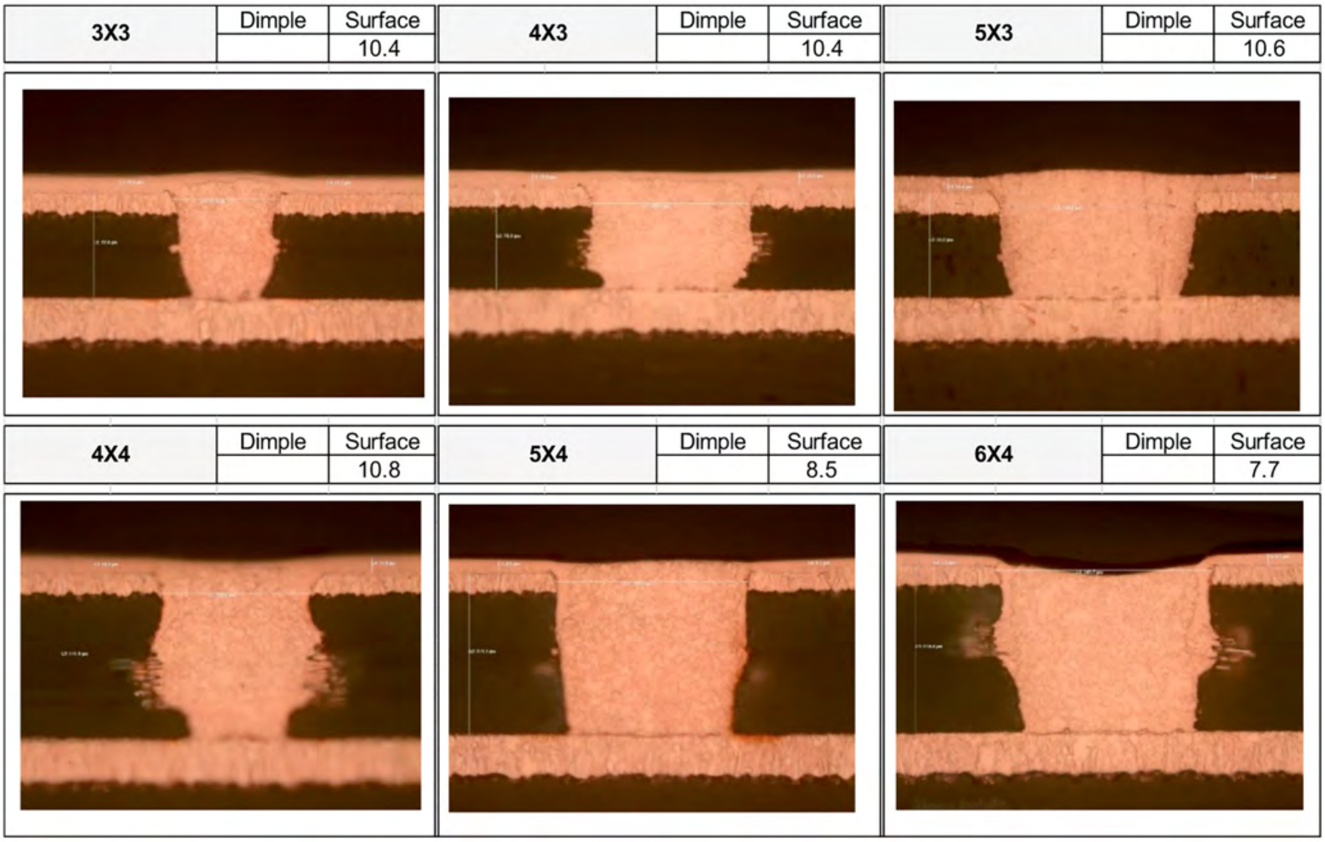


Figure 5: Typical via fill capability for different via diameter and depth at surface copper ~8–11 µm.

observed at very high flow rate. A typical plating was done under the conditions summarized in Table 1 and followed the process flow given above; this resulted in a via fill shown in Figure 5. A via with diameter of 150 µm and depth of 100 µm was seamlessly filled without any issue. Surface was flat, and the deposit was bright with surface copper thickness at only 8 – 11 µm.

Total organic content (TOC) of the bath was obtained for the fresh and aged bath. According to the data summarized in Figure 6, the TOC did not change significantly over time and the fresh bath has very low TOC. Low TOC in the fresh makeup means, the bath will have prolonged lifetime and stability. Since the organic buildup is very low with age, the bath requires less frequent carbon treatment. This makes the process more environmentally benign and hassle-free in terms of waste treatment.

Compatibility of this via fill formulation in direct metallization was evaluated by plating propagation panels. These are panels with

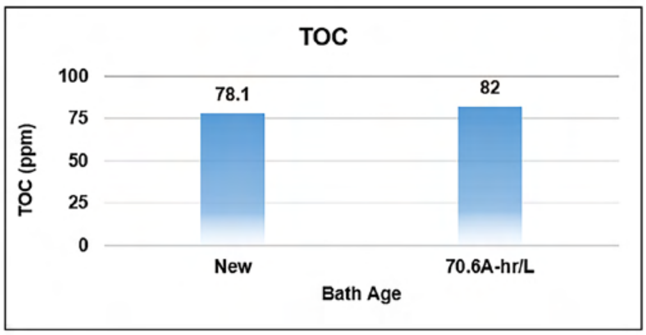


Figure 6: Total organic content of the new bath and aged bath.

eight through-holes alternatively connected and processed with a carbon-based direct metallization layer. Maximum propagation result is eight: two regions for high current density and low current density were plated simultaneously in a Hull Cell. According to the results summarized in Figure 7, the formulation reported here has an excellent propagation at high current density area and low propagation at low current density area.

A 1.6 mm thick through-hole panel was plated to evaluate the micro-distribution. The mi-

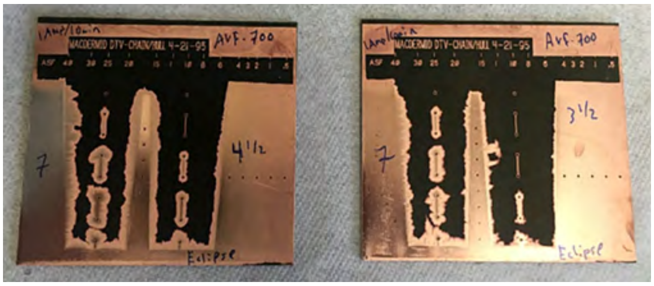
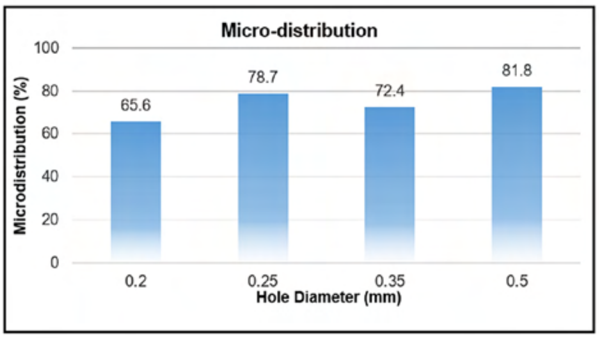


Figure 7: Propagation results for direct metallization applications.

cro-distribution is defined as the ratio of the average copper deposit thickness in the center of the through-hole to the average copper deposit thickness at the surface. According to the data shown in Figure 8, greater than 65% micro-distribution was obtained even in an electrolyte designed for via fill, that is, a high copper and low acid electrolyte. The cross-section evaluation of the through-holes showed no thin corners; however, a sloping was observed from the bulk surface to the through-hole edge.



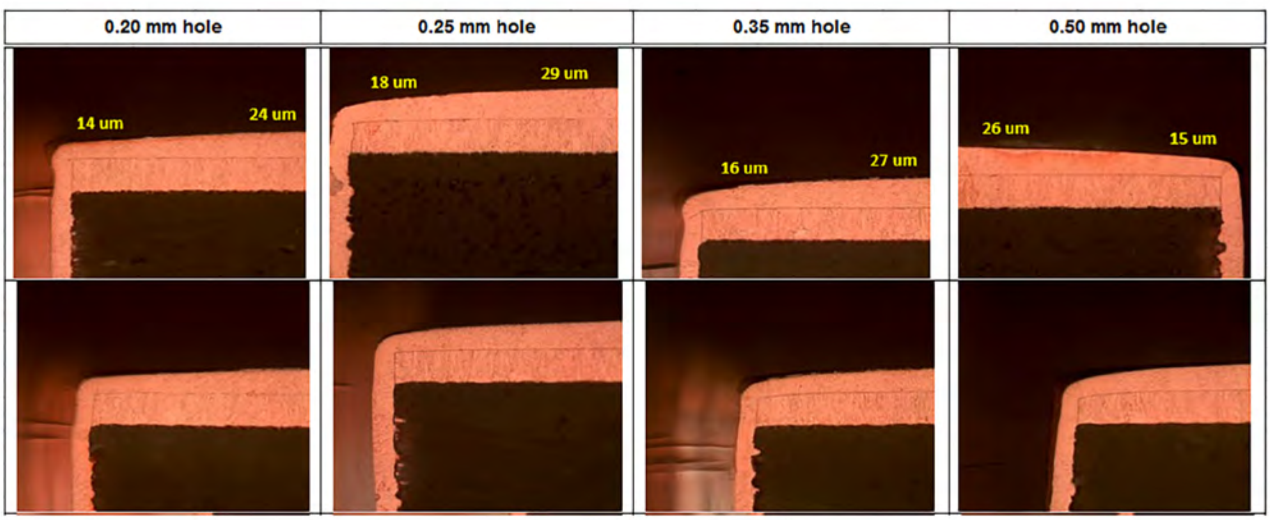


Figure 8: Throwing power for 1.6 mm board thickness. Corresponding micro-distribution shown in graph above.

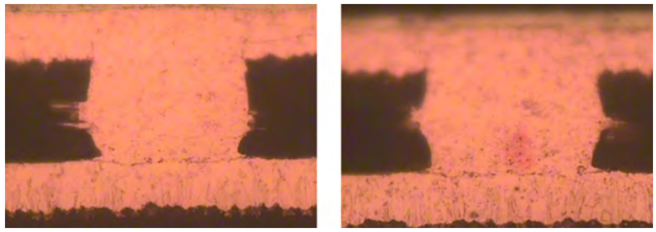


Figure 9: Solder float results.

Further, a solder float test was performed to evaluate thermal characteristics of the deposit in accordance with IPC TM-650 2.6.8. Solder shock (SS) conditions were 10 seconds float at 288°C for three times on the same side of the test coupon. Results are shown in Figure 9. After 3X SS testing, no cracks, or via bottom separation was observed.

Structural Analysis, Hardness and Impurities

X-ray diffraction (XRD) study was performed for the plated deposits to identify the crystal phase and different planes. A typical diffraction pattern (Figure 10) was obtained as the standard reported in the literature with reflections from planes (111), (200), (220), and (311) were observed[8]. Narrow sharp peaks in the XRD pattern were observed which indicates highly ordered copper crystals in the deposit. Table 2 and 3 show no significant change in the major peaks, lattice constant or density of the plated copper after aging. This is an indication that the crystal phase of the deposit is similar even after bath aging up to 150 Ah/L.

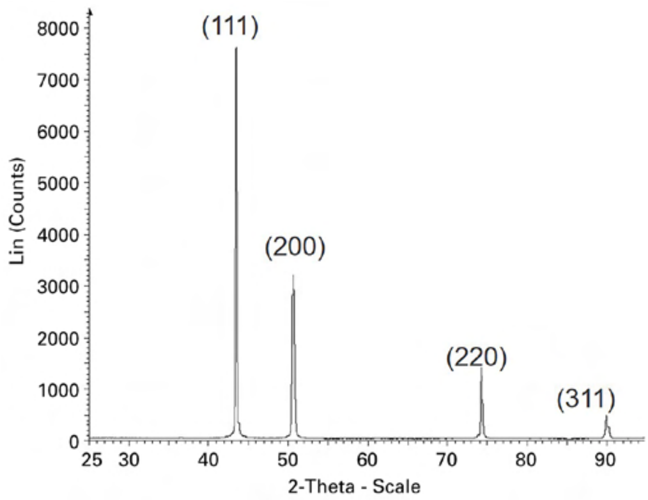


Figure 10: X-ray diffraction pattern for copper deposit plated using current formula.

$$Average\ Crstallite\ Size = \frac{0.94\,\lambda}{\beta\ \cos\theta} \qquad \text{Eq. 2}$$

β = Line broadening at the FWHM in radians
θ = Bragg angle
λ = X-ray wavelength

Tabulated in Table 3 is the crystal size calculated from the full width at half maximum (FWHM) from the XRD peaks using the Scherrer equation (Eq.2). The data show no substantial changes in the crystal size, which agrees with the FIB images in Table 5, showing the grain structure of the plated copper at different bath age. Beside the relative intensities of the crystal orientations, the crystallographic density and the lattice constant is also of interest whether there is a preferred orientation. Lotgering factor needs to be considered to verify this. The Lotgering factor, f, is for each Miller index (hkl) showing whether it is in the range of the thermodynamic stable Miller index distribution for copper (literature values) or which crystal orientation is more preferred up to a certain degree[10]. The calculation of the Lotgering factor for each Miller index is performed according to the following equation (here for the example (00l):

$$f00l = \frac{P00l - P_o}{1 - P_o} \qquad \text{Eq. 3}$$

where P_{001} is the sum of the relative intensities for all (00l) diffractions divided by the sum of the intensities of all (hkl) diffractions ($\Sigma I_{001} / \Sigma I_{hkl}$), and P_O is similarly defined for a randomly oriented sample ($\Sigma I^0_{001} / \Sigma I^0_{hkl}$). The maximum obtainable value for the Lotgering factor is 1. This means that there is a very high preference for this Miller index. Table 4 shows the positive values for (111) plane, indicating that the deposits have a slight preference for (111) plane over others, which is the densest plane of all.

The hardness of the copper foils is independent from the bath age at 79 ± 8 $HV_{0.05}$. Furthermore, up to 150 Ah/L the incorporation of carbon, sulfur, nitrogen and chloride into the copper lattices was investigated. The results are shown in Table 6. Impurity analysis was done as follows: C and S using combustion IR method using production analysis equipment, N by using carrier gas hot extraction (CGHE)

Data	Literature	0 Ah/L	50 Ah/L	100 Ah/L	150 Ah/L
(111)	100	100	100	100	100
(200)	46	28.4	45.7	38.4	35.2
(220)	20	10.4	12	14.6	10.5
(311)	17	8.4	9.9	8.3	7.6
Lattice Constant [Å]	3.615	3.613	3.611	3.613	3.613
Density [g/cm^3]	8.92	8.953	8.963	8.952	8.948

Table 2: X-ray diffraction data of the deposit at different bath age.

Panasonic

Ultra-low Transmission Loss Multi-layer Circuit Board Materials for ICT Infrastructure Equipment

MEGTRON7

Laminate **R-5785(N)**
Prepreg **R-5680(N)**

H-VLP2 Cu and Low Dk Glass-Cloth Specifications

Features

- H-VLP2 copper foil and Low Dk glass-cloth allows for 30% loss improvement than MEGTRON 6
- Glass transition temperature (Tg): 200°C (DSC)
- Reduce process cost (Improve drill processability and ENIG (Electro-Nickel Immersion Gold))

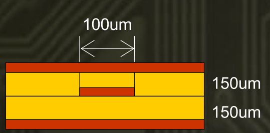
	Dk	Df
R-5785(N) + H-VLP2 Cu	3.4	0.002 @ 12GHz
R-5775	3.6	0.004 @ 12GHz

Applications

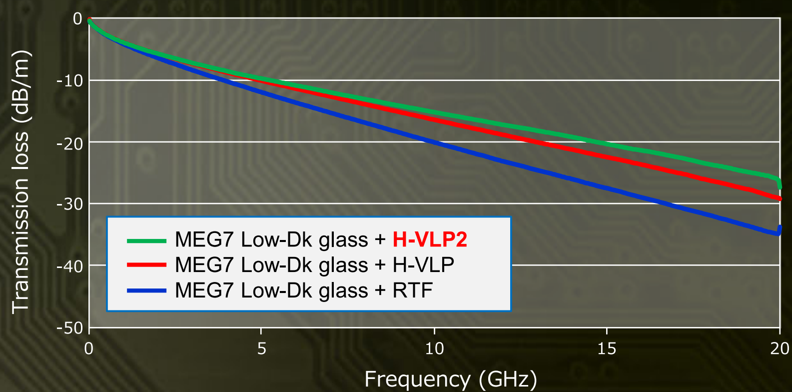
- High-end servers, High-end routers, Supercomputers, and other ICT infrastructure equipment, Antenna (Base station, Automotive millimeter-wave radar), etc.

Trasmission Loss

- Evaluation Sample



Line Length	1000 mm
Impedance	50 Ω
Copper Thickness	18 µm
Inner Cu Treatment	No-surface Treatment
Core Type	#1078 (RC67%) x 2ply
Prepreg Type	#1078 x 2ply



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Crystal plane	Crystal Size [Å]			
	0 Ah/L	50 Ah/L	100 Ah/L	150 Ah/L
(111)	373.1	368.4	371.5	376.3
(200)	308.0	302.7	305.9	309.1
(220)	283.6	282.8	287.6	291.8
(311)	314.6	291.7	304.3	315.5

Table 3: Crystal size of the deposit at different bath age.

Crystal plane	Lotgering Factor			
	0 Ah/L	50 Ah/L	100 Ah/L	150 Ah/L
(111)	0.29	0.11	0.16	0.23
(200)	-0.08	0.03	-0.02	-0.03
(220)	-0.04	-0.12	-0.02	-0.05
(311)	-0.04	-0.04	-0.05	-0.05

Table 4: Lotgering factor at different bath age for different XRD peaks.

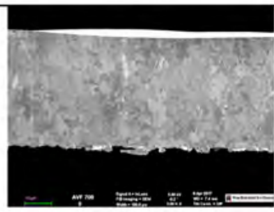
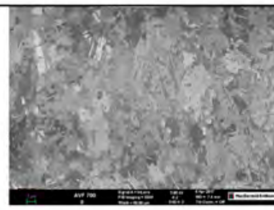
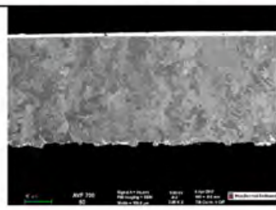
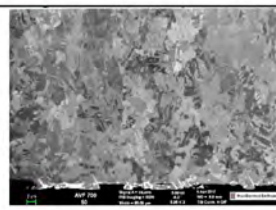
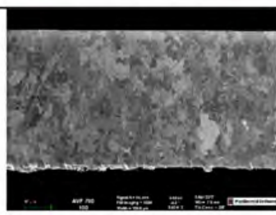
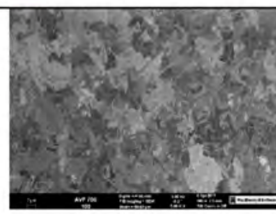
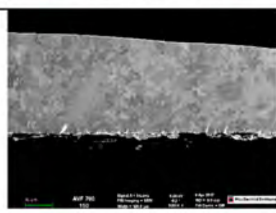
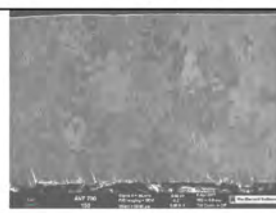
Bath Age (Ah/L)	3 kx	5 kx
0		
50		
100		
150		

Table 5: Grain structure of the deposit over bath age.

Sample	C [% w/w]	S [% w/w]	N [% w/w]	Cl [% w/w]
Product A_0	0.008	< 0.002	< 0.002	< 0.05
	0.005	< 0.002	< 0.002	< 0.05
Product A_50	0.005	< 0.002	< 0.002	< 0.05
	0.004	< 0.002	< 0.002	< 0.05
Product A_100	0.007	< 0.002	< 0.002	< 0.05
	0.007	< 0.002	< 0.002	< 0.05
Product A_150	0.006	< 0.002	< 0.002	< 0.05
	0.006	< 0.002	< 0.002	< 0.05

Table 6: Impurity analysis over bath age.

and for Cl, X-ray fluorescence spectroscopy (XRF spectroscopy).

Beside carbon, no other non-copper elements were detected. Carbon is being incorporated only in very small quantities. No significant increase in carbon content was observed as the bath aged.

Physical and Thermal Properties

The two most important physical properties for PCB manufacturing are tensile strength and elongation %, these properties show the tolerance of the deposit for thermal stress. The copper deposit plated with additives suppressor, grain refiner, and leveler will show characteristic physical properties.

$$\text{Mean average cross sectional area (in2)} = \frac{\text{Weight of the sample (lbs)}}{\text{Length of tensile sample (in)x density of copper (g/in3)}} \quad \text{Eq. 4}$$

$$\text{Tensile Strength} = \frac{\text{Maximum load (lbs)}}{\text{Mean cross sectional area (in2)}} \quad \text{Eq. 5}$$

$$\text{Elongation} = \frac{\text{(Length at break − Original gage length)}}{\text{Original gage length}} \, x\, 100\% \quad \text{Eq. 6}$$

Tensile strength and elongation were measured according to the IPC TM-650, 2.4.18.1 test method standard. A stainless-steel panel was plated with the current formulation. Sample strips were extracted from the plated panel and baked in an oven at 125°C for four to six hours. A production mechanical property test instrument was used to test the strips. The measurements were used to calculate tensile strength and elongation % using equations 4, 5, and 6. Figure 11 shows the results at two different bath ages, fresh bath and bath age around 62 Ah/L. According to the results, properties improved with the bath age.

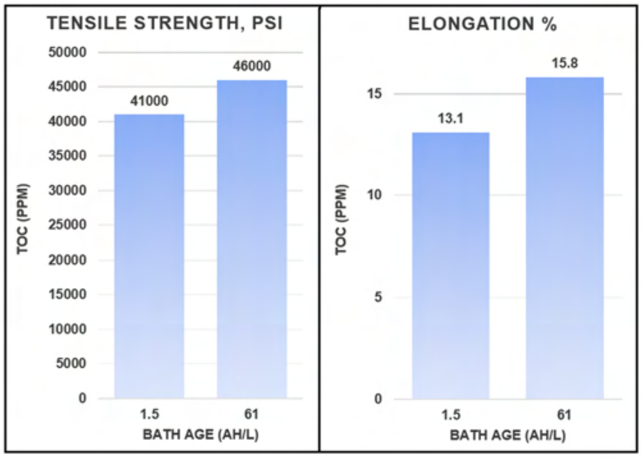


Figure 11: Tensile strength and elongation of the plated deposit.

Conclusions

In summary, a new via fill chemistry is introduced in this paper. The formulation showed excellent via fill capability, with minimum surface copper. Over bath age, very low TOC was observed and insignificant foreign element uptake in the copper deposit was observed. Evaluation of structure showed stable crystal structure during aging, with a slightly preference on the (111) plane. The hardness of the plated deposit was 79 ± 8 $HV_{0.05}$ regardless of the bath age. The physical properties, tensile strength and elongation improved as the bath aged. All the additive components can be analyzed using CVS analysis. PCB007

References

1. Clyde F. Coombs Jr., *Printed Circuit Handbook, Sixth Edition,* McGraw-Hill, New York, 2008.

2. Mordechay Schlesinger, Milan Paunovic., *Modern Electroplating,* Fifth edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2010.

3. W.P. Dow, M.Y. Yen, W.B. Lin, S.W. Ho, "Influence of Molecular Weight of Polyethylene Glycol on Microvia Filling by Copper Electroplating," *Journal of The Electrochemical Society,* 152 (11) C769-C775 (2005).

4. W.P. Dow, C.W. Liu, "Evaluating the Filling Performance of a Copper Plating Formula Using a Simple Galvanostat Method," Journal of The Electrochemical Society, 153 (3) C190-C194 (2006).

5. P. Broekman, A. Fluegel, C. Emnet, M. Arnold, C. Roeger-Goepfert, A. Wagner, N.T.M. Hai, D. Mayer, "Classification of Suppressor Additives Based on Synergistic and Antagonistic Ensemble Effects," Electrochimica Acta, Volume 56, Issue 13, 1 May 2011, pages 4724-4734.

6. K. B. Herbert; S. Adhikari; J. E. Houser, *Journal of the Electrochemical Society,* 152 (5) C324-C329, 2005.

7. S. Dharmarathna et. al., "High Throw DC Acid Copper Formulation for Vertical Continuous Electroplating Processes," IPC APEX Expo 2017, San Diego, California, February 14 – 16, 2017.

8. Y. Zhang, G. Ding, P. Cheng, H. Wang, "Numerical Simulation and Experimental Verification of Additive Distribution in Through-Silicon Via during Copper Filling Process," *Journal of The Electrochemical Society,* 162 (1) D62 – D67 (2015).

9. F. Wang, Z. Zhao, N. Nie, F. Wang & W. Zhu, "Dynamic through-silicon-via filling process using copper electrochemical deposition at different current densities," Scientific Reports 7, Article number: 46639 (2017).

10. R. Furushima, S. Tanaka, Z. Kato, K. Uyematsu, "Orientation distribution–Lotgering Factor Relationship in a Polycrystalline Material—as an Example of Bismuth Titanate Prepared by a Magnetic Field," *Journal of the Ceramic Society of Japan,* 118 [10] 921 – 926 (2010).

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RTW CPCA Show: AWP Discusses Whelen Engineering Project Success

Watch the interview here.

At the recent CPCA Show 2018 in Shanghai, Jochen Zeller, vice president of AWP Group, sat for an interview to discuss the challenges impacting wet processing, such as the continuing miniaturization trend leading to finer widths and line spacings. Zeller also explains his perspective on the need for integrated, automated lines in a factory, and how this benefits PCB manufacturers. Other topics include AWP Group's part in Whelen's engineering project, the technology they provided, the challenges encountered, and how they were able to help address those issues.

MilAero Highlights

It's Only Common Sense: Finally, State Dept Shows its Teeth on ITAR ▶

A good friend of mine sent me this article he received in an email from the law firm of Williams Mullins. Read it and weep, ITAR offenders! Law-abiding companies, rejoice.

Testing Todd: AVI–Your Tireless Friend in Final Inspection ▶

The "automation vs. human" debate continues. There are experts with many years of experience performing final inspection with precise detail. This is not debated. However, circumstances change with unpredictable results.

Triangle Labs: Covering the Niche Market of Large Boards ▶

I recently had the opportunity to speak with John-Michael Gray, president of Triangle Labs. We had quite a discussion on their rather unique capability of building large-format PCBs and multilayers—perhaps the largest PCBs in the world.

Tariffs on China Could Harm U.S. Electronics Companies ▶

IPC—Association Connecting Electronics Industries today warned that the Trump administration's plan to impose higher tariffs on goods imported from China could harm many small- and medium-sized U.S. electronics manufacturers that rely on Chinese materials, components and equipment to produce their products.

Combining Strengths Synergistically: PDS and Green Circuits ▶

Power Design Services (PDS) and Green Circuits have just announced their merger. I-Connect007 Publisher Barry Matties recently sat down with Joe O'Neil and Matthew Becker of PDS, along with Ted Park of Green Circuits, to get the full scoop.

ACT Completes Acquisition of ECT ▶

Additive Circuits Technologies LLC (ACT) is pleased to announce the conclusion of a corporate reorganization and the incorporation of assets acquired from EarthOne Circuit Technologies (ECT) and technology advancements for Autonomous Vehicles.

Sustaining F-35 Electronic Warfare systems ▶

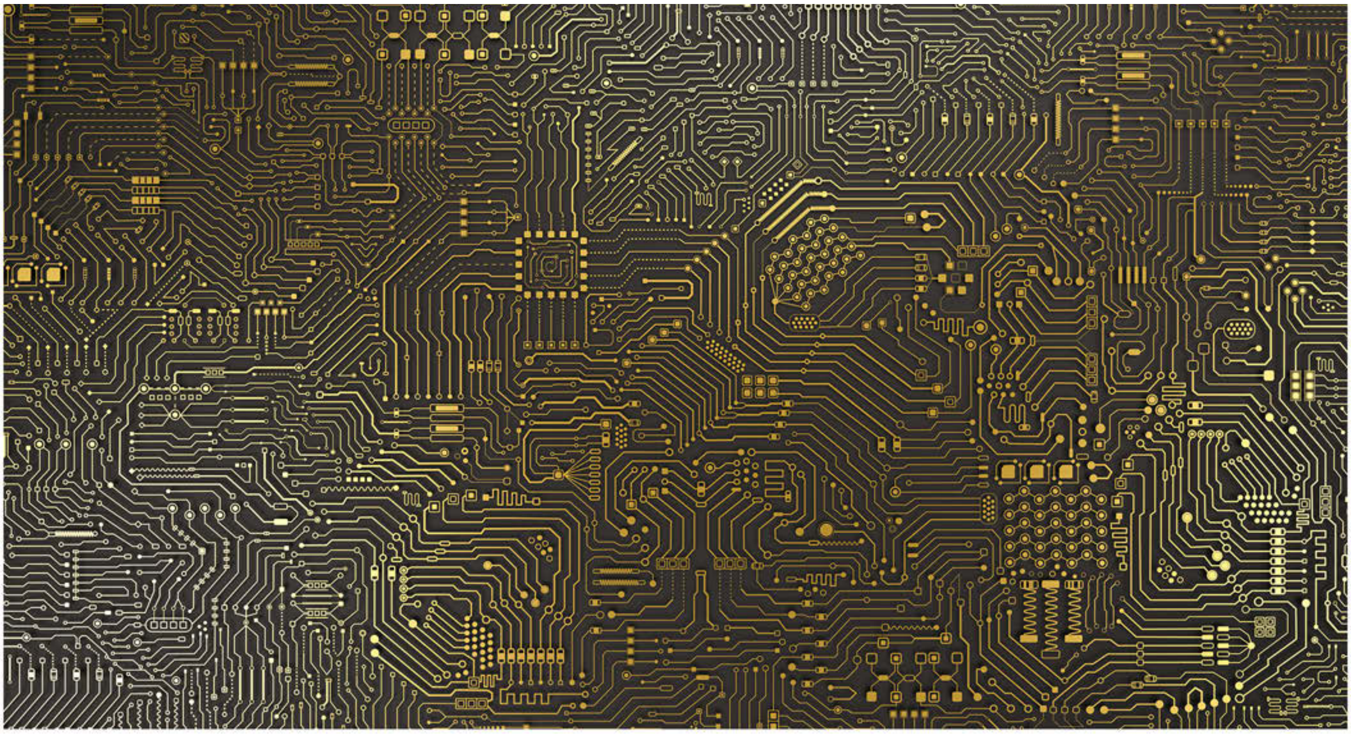
BAE Systems has received a contract from Lockheed Martin to ensure the readiness of critical electronic warfare (EW) systems on the F-35 Lightning II fighter aircraft.

Sparton Teams with Raytheon on Next-Gen Mine Neutralization System ▶

Sparton Corp. will team with Raytheon to support the design, test, and deployment of the next generation Barracuda Mine Neutralization system.

Lasers in Space: Earth Mission Tests New Technology ▶

Imagine standing on the roof of a building in Los Angeles and trying to point a laser so accurately that you could hit a specific building in San Diego, more than 100 miles (160 kilometers) away.



Characteristics of New Electroless Au/Pd/Au Process for Fine-Line Applications

Feature by Tetsuya Sasamura, Ph.D., Tatsushi Someya, Eriko Furuya, Katsuhisa Tanabe, and Shigeo Hashimoto
C. UYEMURA & CO., LTD., HIRAKATA, OSAKA, JAPAN

Abstract

The characteristics of electroless gold/palladium/gold (IGEPIG) deposit, which has been newly developed for fine-line application as electroless nickel-phosphorus (EN) free, has been compared with that of conventional electroless Ni-P/Pd/Au (ENEPIG) deposit and electroless Pd/Au (EPIG) deposit.

The IGEPIG deposit had excellent wire bonding reliability (WBR) compared with other deposits even if the gold thickness of IGEPIG at the top surface was less than that of the EPIG and ENEPIG deposits. From the results of AES analysis after heat treatment for 16 hours at 175°C, Pd and Cu was hardly detected at the top surface of Au, and it indicated that IGEPIG deposit prevented Cu and Pd diffusion. Also, it was revealed by EBSD (electron back scatter diffraction pattern) analysis that Pd grain size on Au was about ten times bigger than those on a Pd-activated copper surface. It was assumed that the prevention of Pd and Cu diffusion was relative with bigger Pd grain size of IGEPIG deposit.

Solder joint reliability (SJR) of IGEPIG deposit with SAC305 (Sn-3.0Ag-0.5Cu) solder ball is better than that of EPIG deposit, and almost the same with that of ENEPIG deposit. IGEPIG deposit had excellent pattern ability, because of no EN deposit and Pd activator process compared with ENEPIG and EPIG.

Introduction

Recently, the pattern of copper lines and spaces on PCBs has become narrower with the miniaturization of the integrated circuit. If using a conventional ENEPIG process with a nickel thickness of 5–6 µm, it will be easy to cause short circuits between each pattern line because of over-plating. Electroless nickel plating grows both vertically and horizontally, thus increasing the chance of bridging traces when the distance between traces is small. Converse-

ly, the electroless palladium and immersion gold plated deposits are normally quite thin which reduces chance of metal bridging.

In addition, there is the requirement for reducing the EN deposit because less electronic signal loss is necessary for RF (radio frequency) module. As an EN-less or EN-free process, the electroless thin Ni/Pd/Au (thin ENEPIG) or EPIG process has been proposed. However, the pattern ability of thin ENEPIG has some restrictions for extremely fine patterns because a Pd activator process is used. In some cases, residual Pd activator (catalyst) could remain between traces, even with thorough rinsing, and help to serve as sites for extraneous metal plating between traces. And the WBR of EPIG after heat treatment (HT) was inadequate, especially when the gold thickness is less than 0.1 µm. The main factor is that WBR becomes worse by HT is Pd and Cu diffusion to the top surface of Au.

After much examination, we developed the IGEPIG process without Pd activator or any EN deposit as a new process which has excellent WBR and pattern ability. In this study, we introduce the performance of the IGEPIG deposit.

All three finishes discussed are wet plating processes, depositing metals from aqueous solutions. ENEPIG utilizes both immersion reactions (palladium catalyst and immersion gold) and electroless reactions (electroless nickel and electroless palladium). EPIG utilizes immersion reactions (palladium catalyst and immersion gold) and one electroless palladium step. IGEPIG utilizes two immersion reactions (an initial immersion gold and final immersion gold) and one electroless palladium step. All three processes utilize the same aqueous chemical pre-treatment of cleaning, copper micro-etching, and acid dipping.

Experimental Methods

The coupons used in this study consisted of a copper-clad laminated substrate which was copper plated to a thickness of 20 µm using an acid copper electroplating process. For SJR tests, the copper-plated substrate was coated with solder mask and imaged to form the solder ball pads of 0.25 mm diameter. Furthermore, the substrate of the copper pattern with 20 µm space of the wiring line was used for evaluating of the pattern ability. Each substrate was plated with EPIG, ENEPIG and IGEPIG by using plating chemicals commercially available from Uyemura. Table 1 shows the plating process of each deposit. For Pd plating of ENEPIG deposit, pure Pd and Pd-P type were compared. And pure Pd type was used for Pd plating of EPIG and IGEPIG.

As the solder ball for the evaluation of SJR, 0.3 mm diameter of Sn-3.0Ag-0.5Cu was used. The reflow profile with the top temperature of

Process	ENEPIG	EPIG	IGEPIG
Cleaner	✔	✔	✔
Soft etching	✔	✔	✔
Acid rinse	✔	✔	✔
Pd activator	✔	✔	---
Immersion Au	---	---	✔(0.02 um)
Electroless Ni	✔(6.0 um)	---	---
Electroless Pd*	✔(0.1 um)	✔(0.1 um)	✔(0.1 um)
Immersion Au	✔(0.1 um)	✔(0.1 um)	✔ (0.08 um)

Total 0.1 um

Table 1: Plating processes of ENEPIG, EPIG and IGEPIG.

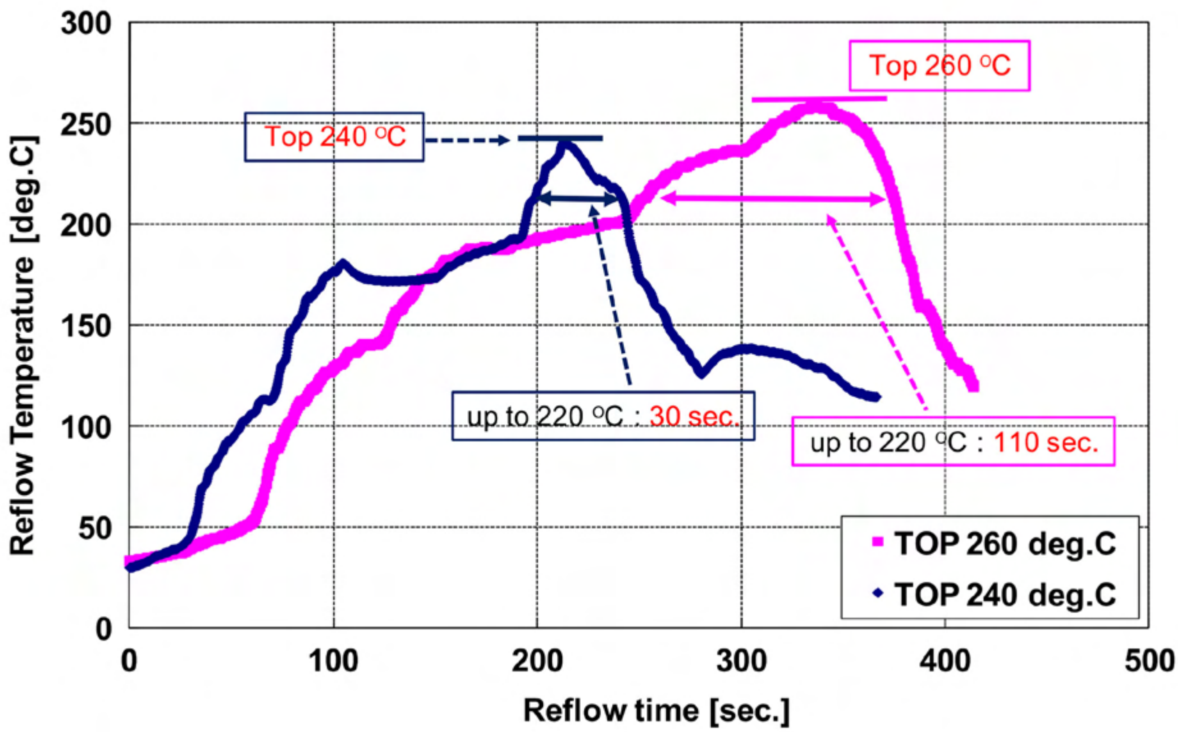


Figure 1: Reflow profiles.

240°C or 260°C was applied for mounting the solder ball as shown in Figure 1. SJR was measured by ball pull (BP) test as shown in Table 2. The cross-section image of the deposits was observed by FIB-SEM. Electroless Ni was plated to protect Au deposit at the top surface before FIB. And the cross-section image of intermetallic compounds (IMC) after mounting the solder ball was observed by FE-SEM after polishing by cross section polisher.

WBR was evaluated by wire bonding and pull test as shown in Table 3. The condition of heat treatment for WBR was done for 16 hours at 175°C.

BP Test Conditions	
Reflow equipment	Tamura TMR-15-22-LH
Reflow environment	Air
Solder ball	SAC305 (M705) / Senju
Solder diameter	0.30 mm
Pad diameter	0.25 mm
Flux	529D-1 (RMA type)/Senju
Reflow conditions	240°C 5 times or 260°C 1, 5 times
CBP test equipment	Dage series 4000
Pull speed	1,000 µm/sec

Table 2: Test conditions of ball pull (BP) test.

The element analysis at the top surface for each deposit was measured by Auger electron spectroscopy. The conditions of AES are shown in Table 4.

Inverse pole figure (IPF) image of the cross-section for each deposit was observed using

Wire bonding test conditions	
Equipment	TPT HB16 (semi-auto bonder)
Capillary	B1014-51-18-12 / PECO
Wire	1.0 mil-gold (GFC) / TANAKA
Temp.	150 deg.C
Step	0.7 mm
1st bonding conditions	Ultra sonic = 250 mW Time = 200 msec Force = 25g
2nd bonding conditions	Ultra sonic = 250 mW Time = 50 msec Force = 50g
Pull test equipment	Dage series 4000
Pull speed	170 µm/sec

Table 3: Test conditions of wire bonding.

AES conditions	
Equipment	JEOL 9500F
Ep	10 keV
Ip	4×10^{-8} A
Area	120 µm x 120 µm
Tilting Angle	30°

Table 4: AES conditions.

EBSD conditions	
Equipment	TSL OIM 7.0
	EDAX DigiView 5
SEM equipment	JEOL JSM-7800F
Accelerating voltage	15 kV
Tilting Angle	70°
Step size (IPF image)	0.05 µm
Step size (Grain size calculation)	0.01 µm (Pd for EP), 0.05 µm (Pd for IGEP), and 0.15 µm (Cu)
Grain tolerance angle	5°

Table 5: EBSD conditions.

FE-SEM equipped with OIM (orientation imaging microscopy) system of EBSD after polishing by CP and carbon coating. EBSD conditions are shown in Table 5.

Results and Discussion

Pattern Ability

The ability to plate fine patterns is demanded for most of today's boards and packages. While electroless nickel plated layers serve as an excellent diffusion barrier to copper, limits are being seen for deposit thickness in many of the new board designs. Figure 2 shows the comparison of plating pattern ability between IGEPIG, EPIG, and ENEPIG deposits with pure

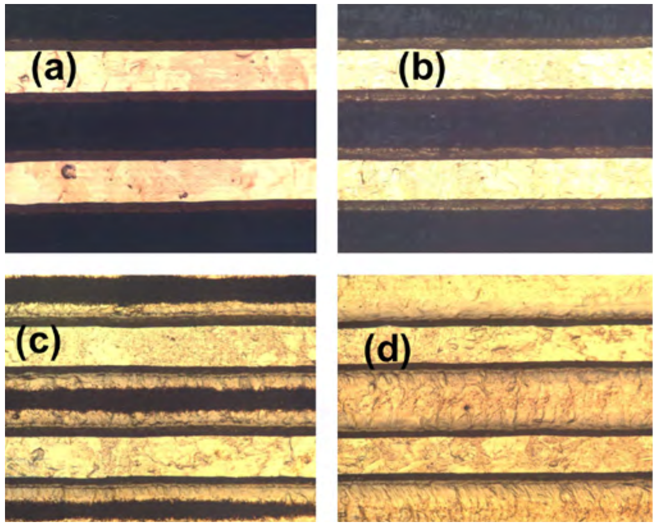


Figure 2: Optical microscope image of fine line pattern with L/S=30 µm/20 µm (a) before plating, (b) after IGEPIG plating, (c) after EPIG plating, (d) after ENEPIG plating.

Pd. Although ENEPIG process had over-plating in the space of the wiring line and a little over-plating was observed for EPIG deposit, no over-plating was observed for IGEPIG deposit. It seemed that the thickness of EN deposit was main factor of over-plating while the Pd chemical activator process also had some influence. Because IGEPIG process has no electroless nickel and activator process, the pattern ability was excellent compared to the others.

Solder Joint Reliability

For the evaluation of SJR for each deposit after mounting the solder ball, BP was evaluated by the failure mode after pulled the solder ball as shown in Figure 3. Points were assigned to four types of failure mode. For complete broken case in the solder ball, 5 points were assigned. If the broken interface contained less than 25% IMC, 2.5 points was assigned. Final-

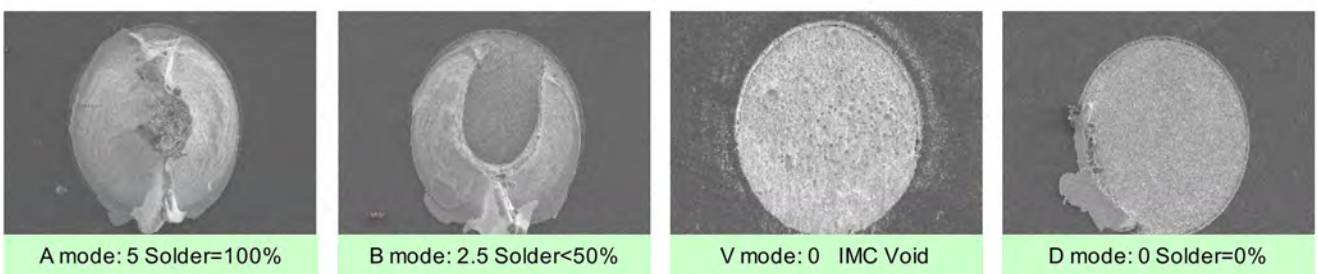


Figure 3: Failure mode of BP and BP point for each ball.

Reflow Peak Temperature	240°C	260°C	
Number of Reflow Cycles	5	1	5
ENEPIG with Pd-P	100	100	100
ENEPIG with pure-Pd	100	100	23
EPIG	100	0	0
IGEPIG	100	100	32

Table 6: Ball pull points of each deposit.

ly, if the broken interface contained more than 25% IMC or voids, zero points was assigned. For example, if all 20 balls were broken completely at the solder without IMC appearance, total point results equal 100 since five points were assigned for each ball.

Total BP points are shown in Table 6 for each deposit and each reflow condition. For ENEPIG deposit with Pd-P, BP points were 100 even when the reflow condition was 5x at 260°C, which condition is too severe and usually not required. IGEPIG and ENEPIG with pure Pd deposits were also 100 except for 5x reflow at 260°C. The important thing is that SJR of IGEPIG was almost same with that of ENEPIG with pure Pd, which is entirely acceptable for industry, and was better than that of EPIG deposit.

The cross-section image of IMC was observed to consider difference of SJR when reflow condition was one time at 260°C. From IMC observation results of Figure 4, $(Cu, Ni)_6Sn_5$ was formed as layer 1 and $Ni + Ni_3P$ was formed near Ni-P layer as layer 2 when ENEPIG deposit was used both with Pd-P or pure Pd[1, 2,3]. On the other hand, Cu_6Sn_5 was formed as layer 1 and Cu_3Sn was formed near Cu layer as layer 2 when EPIG or IGEPIG deposit was used[4]. IMC which formed from ENEPIG deposit was

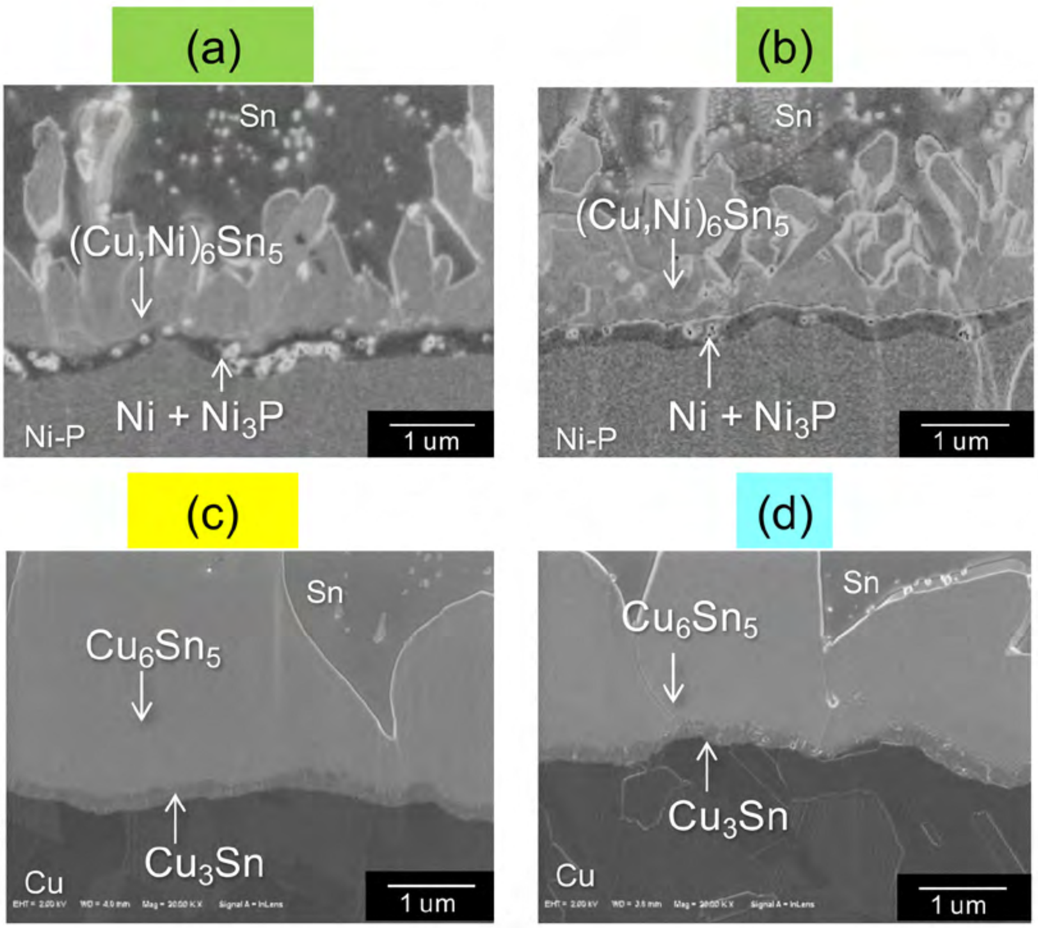


Figure 4: Cross-section image of IMC; (a) ENEPIG with Pd-P, (b) ENEPIG with pure Pd, (c) EPIG, and (d) IGEPIG, one time reflow at 260°C.

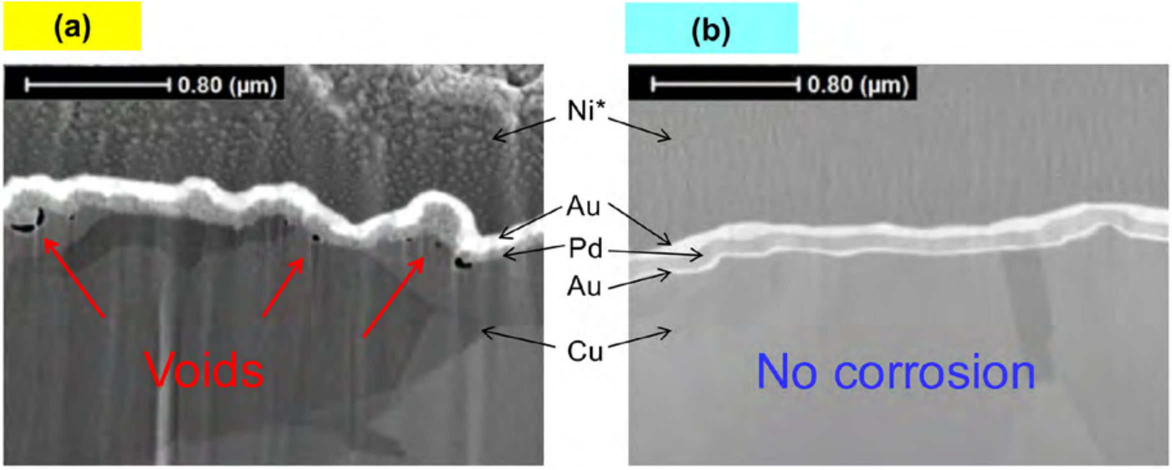


Figure 5: Cross-section image by FIB-SEM; (a)EPIG, (b) IGEPIG; *Ni; protecting layer of Au layer during FIB.

thin and uniform compared with that in case of IGEPIG and EPIG. It seemed that this thin and uniform IMC resulted in excellent SJR. The difference of SJR for P contents in EP layer for ENEPIG deposits had already reported[5].

The cross-section images of deposits before mounting solder ball were also observed as shown in Figure 5 to consider the difference of EPIG and IGEPIG. A lot of voids were observed between Pd layer and Cu for EPIG deposit. On the other hand, it is difficult to confirm any voids in this magnification for IGEPIG deposit. Generally, voiding between copper and plated metal is influenced by copper surface roughness, the type of electrolytic copper, the kind of palladium activator, soft etching, etc. It was assumed that the palladium activator process caused these voids because this process is a displacement reaction with copper and these voids had some worse influence for SJR of EPIG deposit, compared with that of IGEPIG deposit.

Wire Bonding Reliability

WBR was evaluated by pull strength of gold wire pull test for the sample as plated and after heat treatment as shown in Table 7. For the sample as plated, wire pull strength of EPIG, ENEPIG and IGEPIG deposits were all sufficient. For the sample after heat treatment (HT) for 16 hours at 175°C, wire pull strengths of EPIG and ENEPIG deposits decreased. On the other hand, though the strength for IGEPIG deposit became slightly worse after HT, the value was still sufficient and comparable to ENEPIG and EPIG deposits without heat treatment (the sample as plated).

The wide scans of AES were measured at the top Au surface of each deposit after HT as shown in Figure 6 to understand the difference of pull strength of Au wire. Though Pd for ENEPIG, Cu and Pd for EPIG were detected, these metals were not detected for IGEPIG deposit. The ratio of Pd, Cu, Ni, and Au intensity at Au surface after HT for each deposit was calculated from AES results as shown in Figure 7. Obviously, IGEPIG deposit prevented Cu and Pd diffusion. The comparison between EPIG and ENEPIG showed EN barrier prevent Cu diffusion. Wire bonding reliability related with the Au ratio at the top surface of each final finishing. Because Au ratio of IGEPIG was quite high even if it was after heat treatment, IGEPIG deposit had better potential of WBR than

Pull strength for each process (g)		
Process	As plated	After HT*
ENEPIG with Pd-P	9.6	7.6
ENEPIG with pure Pd	9.7	7.9
EPIG	10.7	6.4
IGEPIG	10.9	10.1

Table 7: Pull strength of gold wire for each deposit, before and after heat treatment for 16 hours at 175°C.

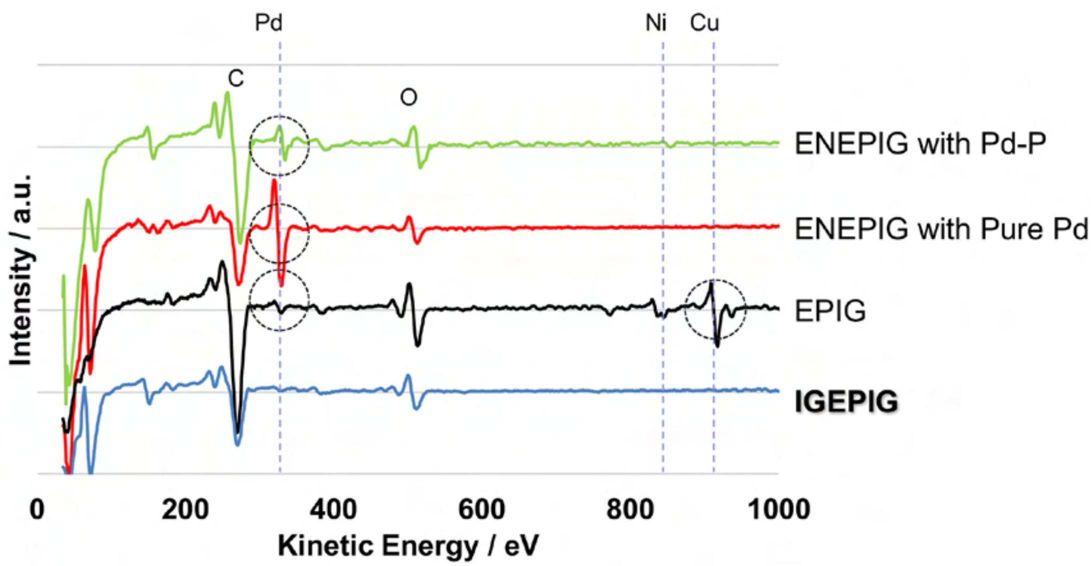


Figure 6: Wide scan results of AES for each deposit after 16 hours at 175°C.

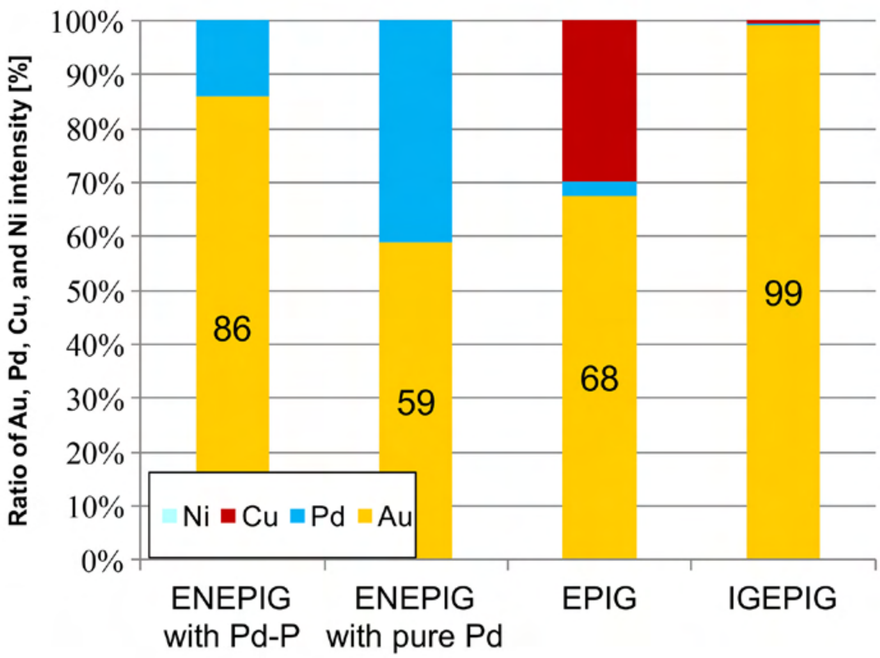


Figure 7: Ratio of Pd, Cu, Ni, and Au intensity at the top surface for each deposit after 16 hours at 175°C.

ENEPIG deposit. It was assumed that Pd layer of IGEPIG had some difference with that of EPIG because there was the different degree of Pd diffusion between EPIG and IGEPIG. So, as next step, Pd layer itself was focused for IGEPIG and EPIG deposit.

When the cross-section image of EPIG and IGEPIG deposits were compared by FIB-SEM which Pd was thicker as shown in Figure 8, and the grain size of Pd layer for IGEPIG seemed to be much bigger than that for EPIG. For EBSD analysis, IGEP (Au/Pd) and EP (Pd) on Pd activator were utilized instead of IGEPIG and EPIG deposit. SEM image and the colors of inverse pole figure (IPF) image which shows crystal orientation of each metal (vertical plane) were compared at same magnification in Figure 9. It was easy to distinguish the interface between Pd and Cu from SEM images. However, it was difficult to distinguish the

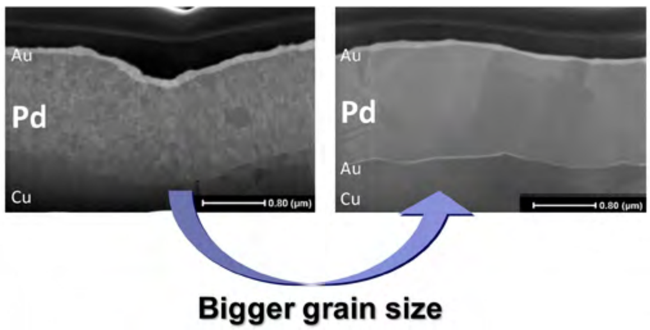
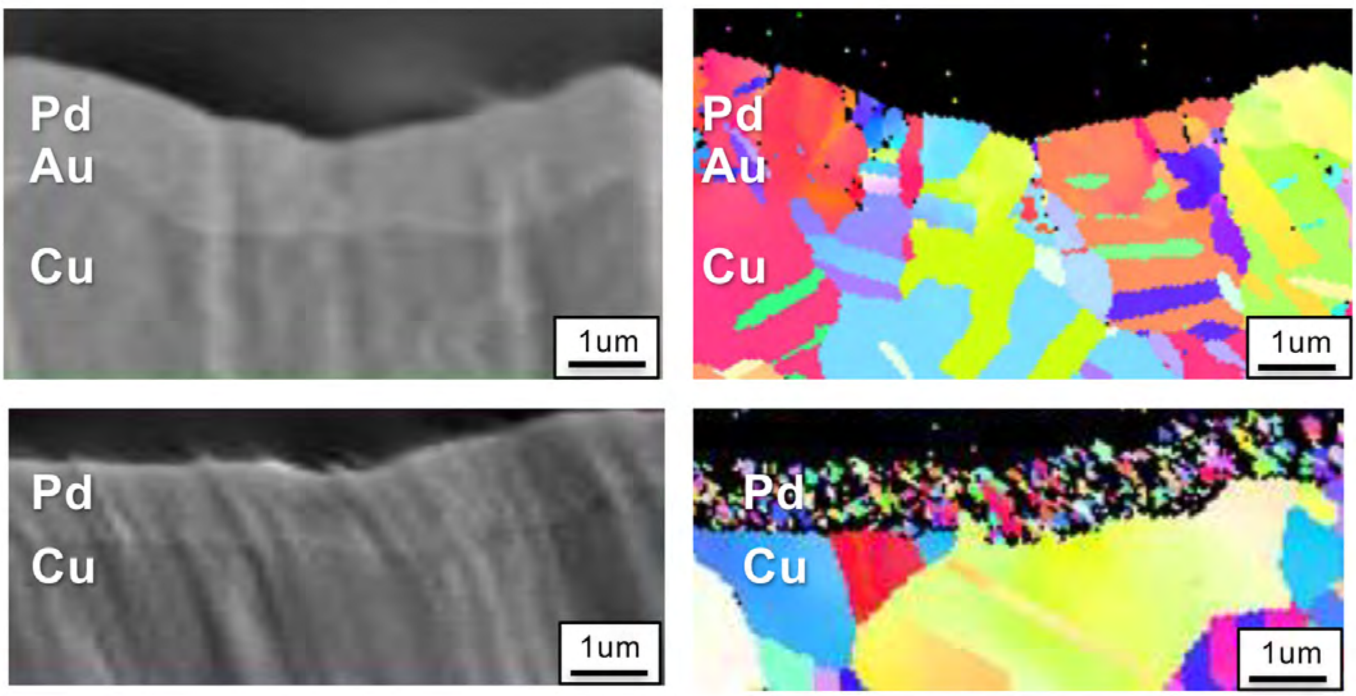


Figure 8: FIB-SEM image; (a) EPIG with 1.2 μm Pd, (b) IGEPIG with 1.2 μm Pd.

interface between Cu and Pd from IPF image for IGEP deposit, which Pd area had partially same color with Cu area. Obviously, it indicated that Pd crystal orientation grew along with that of Cu for IGEP deposit. This may relate with the crystal lattice that Cu, Au, and Pd are face-centered cubic (FCC). The gold layer of IGEP deposit was too thin to observe in this EBSD condition, which the sample tilt was 70 degrees and the accelerating voltage and irradiation current of this condition are higher than those of high resolution conditions.

On the other hand, Pd grain size was very small for EP deposit which Pd layer deposited from palladium activator on copper and this crystal orientation of Pd grain was random. It was very difficult to analyze EBSD pattern because the grain size was small. So, there were a lot of black parts in IPF image of EP deposit. The average grain size of Cu as under layer was around 0.7 μm from the calculation by EBSD analysis, which grain boundaries was defined as more than 5 degrees. The average grain size of Pd deposit on Au layer was about 0.34 μm, which had same order with Cu grain. However, Pd grain size which deposited from Pd activator on copper was less than 0.045 μm which is an order less than that of Cu. It means the Pd layer did not grow along with Cu structure. In the case of ENEPIG with pure Pd, because Ni-P layer is known as an amorphous



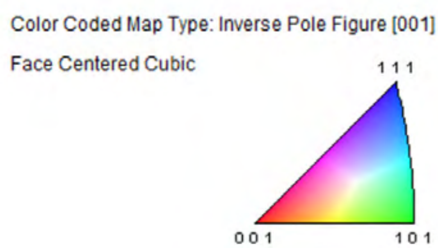
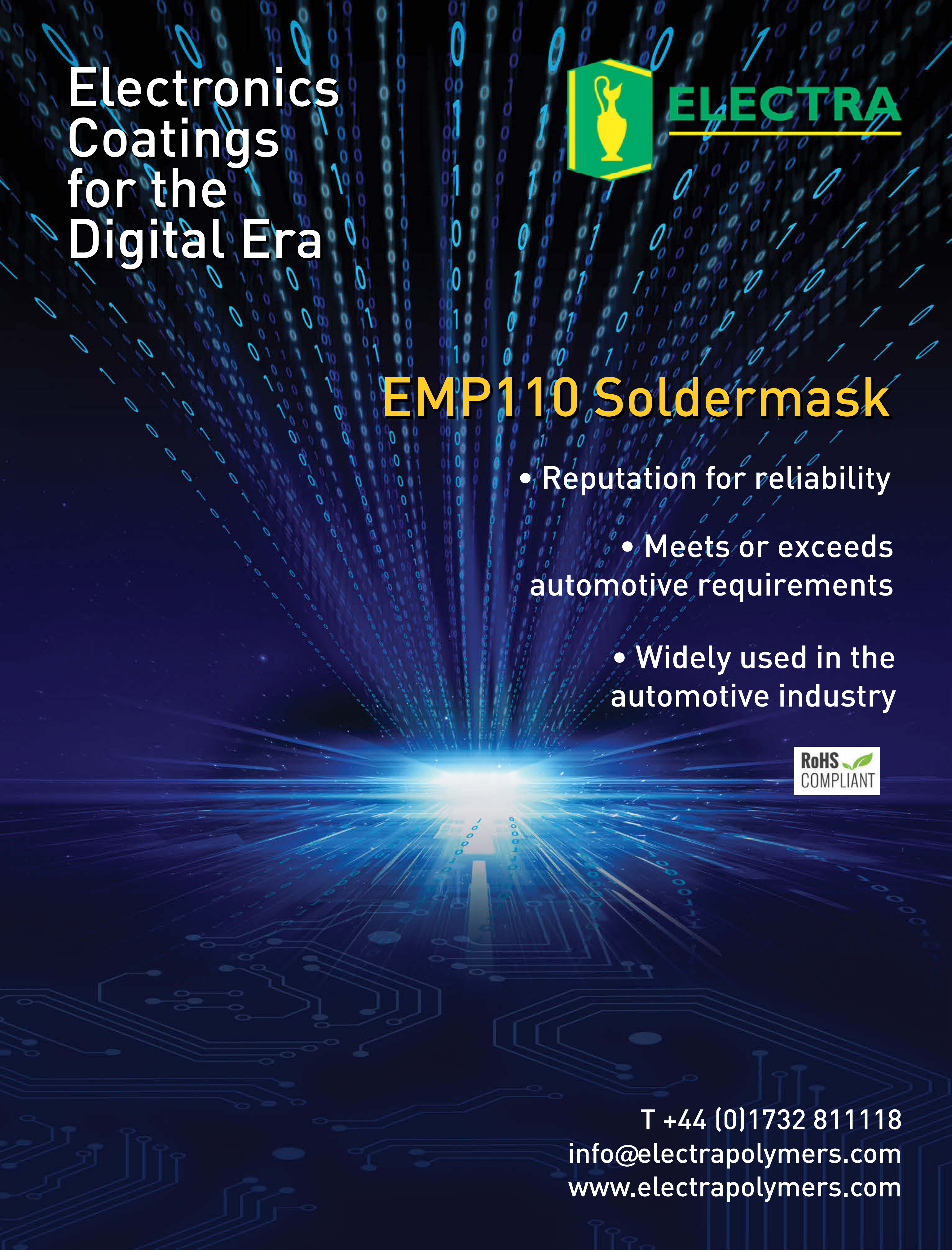


Figure 9: EBSD results; (a) SEM image of IGEP, (b) IPF image of IGEP, (c) SEM image of EP on Pd activator, (d) IPF image on Pd activator, (e) color-coded map of IPF images.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structure, the Pd grain size of the Pd layer also seemed to small size. From these results, it was thought that Au on Cu and Pd on Au deposited as epitaxial growth along with crystal orientation of under layer, and this fact resulted in bigger Pd grain on IG.

Process	Evaluation item		
	Pattern ability	SJR	WBR
ENEPIG with Pd-P	poor	excellent	good
ENEPIG with pure Pd	poor	better	good
EPIG	good	good	poor
IGEPIG	excellent	better	excellent

Table 8: Conclusions of the testing.

WBR of IGEPIG was more superior to that of other conventional process. The superiority of WBR came from prevention of Cu and Pd diffusion to the top surface of Au from the AES results. EBSD analysis revealed that Pd grain size of IGEPIG was quite bigger than that of EPIG and Pd crystal orientation of IGEPIG was same with that of Au on Cu and Cu itself. It seemed that Au on Cu and Pd on Au were formed as epitaxial growth along with Cu crystal orientation of under layer. For IGEPIG deposit, it was assumed that the prevention of Pd and Cu diffusion came from bigger Pd grain size of IGEPIG deposit and resulted in excellent WBR even if after HT.

Because Pd grain size depends on the crystal structure of Cu, it will be necessary to investigate the influence of electrolytic Cu type, grain size of Cu, the condition of etching and Au plating bath condition on Cu, and so on.

Conclusions

The IGEPIG process had better pattern ability for narrow spaces, compared with the conventional ENEPIG and EPIG process because of the elimination of EN and Pd activator process. IGEPIG deposit indicated excellent WBR after HT for 16 hours at 175°C, compared with EPIG and ENEPIG deposits, even if Au thickness of IGEPIG at the top surface was same with that of EPIG and ENEPIG deposits (Table 8).

From the results of AES analysis after HT, it was confirmed that no Pd or Cu was detected at the top surface of Au when using IGEPIG deposit, although Pd or Cu diffusion was detected when using EPIG or ENEPIG deposit. At same time, the mechanism which Pd diffusion prevention was relative with bigger Pd grain size was clarified by using cross sectional EBSD. Additionally, SJR of the IGEPIG deposit was almost same with that of ENEPIG with pure Pd and was better than EPIG deposit when using Sn-3.0Ag-0.5Cu as solder ball. **PCB007**

References

1. Donald Gudeczauskas et al., 39th International Symposium on Microelectronics, October 8–12, 2006, San Diego, California.
2. V. Vuorinen, T Laurila, H. Yu, and J. K. Kivilahti, J. Applied Physics, 99, 023530 (2006).
3. Yukinori Oda, Masayuki Kiso, Akira Okada, Kota Kitajima, Shigeo Hashimoto, George Milad, Don Gudeczauskas, 41st International Symposium on Microelectronics, Providence, Rhode Island, Nov (2008).
4. Shigeo Hashimoto, Katsuhisa Tanabe, Masayuki Kiso, Kota Kitajima, Tatsushi Someya, Don Gudeczauskas and George Milad, SMTA International Conference Proceedings, 2013.
5. Tsuyoshi Maeda, Shinsuke Wada, Katsuhisa Tanabe, Yukinori Oda, Shigeo Hashimoto, Don Gudeczauskas and George Milad, SMTA International, 2015.

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Katsuhisa Tanabe is department manager, final finish;
Shigeo Hashimoto is senior managing director, all with C. Uyemura & Co.

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PTH Failure Mechanisms and Using IST as a Tool, Part 1

Trouble in Your Tank

Feature Column by Michael Carano, RBP CHEMICAL TECHNOLOGY

Introduction

Getting to the root cause of a defect is not a simple task. As stated numerous times in these columns over the last several years, a defect may have its genesis in a process or processes several steps removed from the operation where the defect manifests itself. This edition of "Trouble in Your Tank" will elucidate the difficulty of root cause defect analysis when incorrect assumptions (and thus conclusions) are made. Further, I will illustrate that when proper tools are used to study the issue, additional data is gathered that supports the actual cause of the defect.

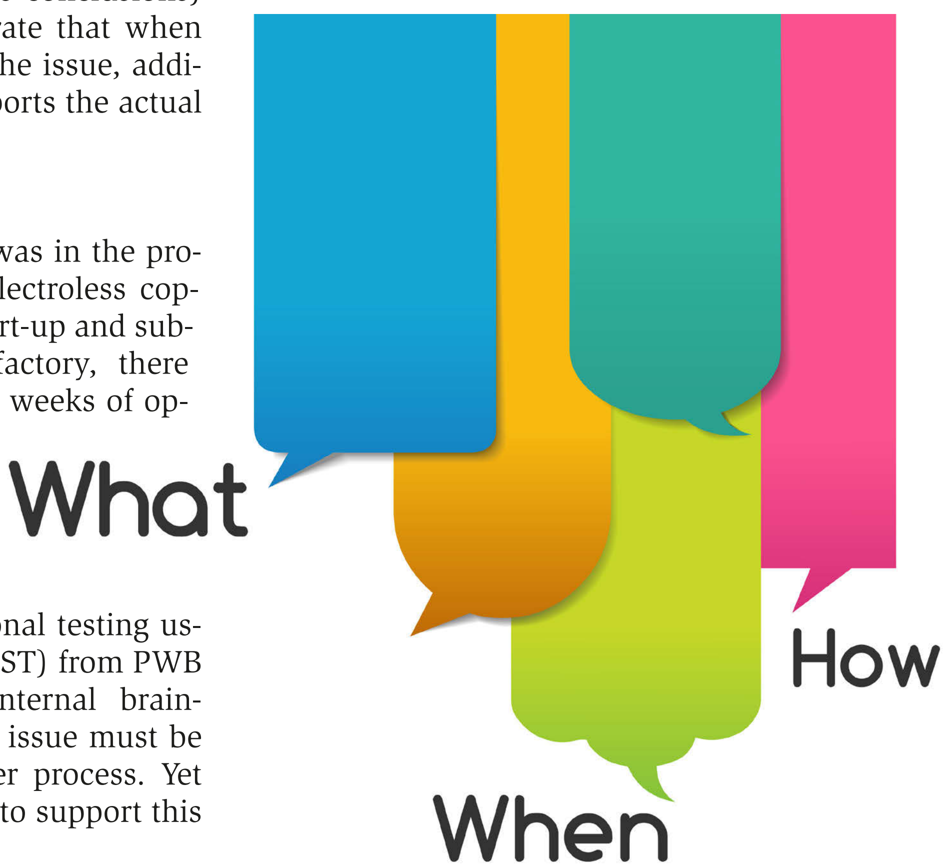
The Issue

In this instance, a fabricator was in the process of evaluating a different electroless copper process. While the initial start-up and subsequent production was satisfactory, there was a defect noted after several weeks of operation. At first, in-circuit test (ICT) found an open. Cross-sectioning revealed a fracture in the electroplated copper after solder float. The fabricator then decided to perform additional testing using interconnection stress test (IST) from PWB Interconnect Solutions. The internal brainstorming team strongly felt this issue must be related to the electroless copper process. Yet there was no concrete evidence to support this theory.

What follows is a systematic procedure to get to the root cause of the problem. But first, a bit of background on IST.

IST Testing and Mechanism

IST has been a standard failure analysis method in the industry for over two decades. IST is a tool that provides insight into PWB failure mechanisms and allows fabricators and



chemistry/material suppliers to make improvements in the fabrication process to enhance long-term reliability. These improvements are not exclusive to process and materials as design of the PWB may also contribute to failure.

IST has both the capability of effectively and rapidly quantifying the integrity of the plated through-hole (PTH) and the unique ability to identify the presence and levels of post separation within the multilayer board (MLB)[1]. A typical IST coupon has two circuits typically designed into the coupon: a power circuit for direct heating through the interconnect and a sensing circuit to measure stress and strain in the barrel of the PTH.

This test method measures cycles to failure on these specially designed IST coupons that are thermally cycled using current flow through internally heated circuits that heat the coupon and the adjacent plated-through holes. Failure is defined as a 10% increase in the resistance of the PTH[2].

In short, there are any number of factors that can precipitate the failure of either the electroless copper-to-post interconnect, or the failure of the electroplated copper in the via itself. In terms of failure in the plated-through hole or the post interconnect, thermal excursions are the major cause of failures. Figure 1 depicts a schematic of key defects in the plated through-hole that are thermally induced.

The primary cause of barrel cracking is the CTE mismatch between the resin matrix and the electrodeposited copper. This is taking place in the Z-axis. Movement in the X-Y plane is somewhat more restricted than in the Z-axis due to the glass fiber reinforcement. In addition, the resin CTE increases sharply above its glass transition temperature, causing further CTE mismatch strain induction on the copper and the potential for PTH/PTV failure.

With all this information, where does the fabricator go from here? Certainly, using higher Tg, lower CTE materials would be a benefit for improved reliability. But at what added material cost? In addition, a change in material will certainly impact other aspects of the board including electrical functionality that may not be acceptable to the end user.

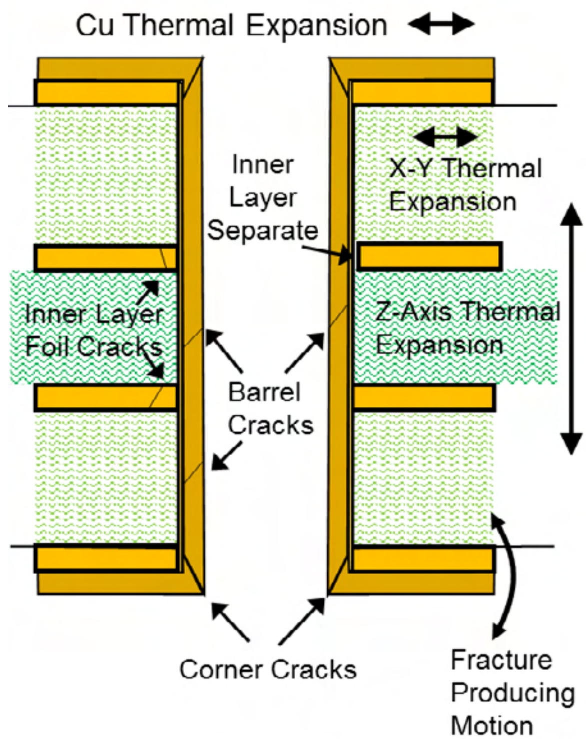


Figure 1: Common failure mechanisms in plated through-holes. (Source: IPC Wisdom Wednesday presentation, July 2017)

Interconnect defects (ICD)—that is, the separation of the plated copper (either electroless or electrolytic) from the post innerlayer—is a different failure mechanism than described above. The good news is that IST testing can differentiate between barrel cracking failures and ICD failures. The bad news is these are both failures. However, understanding what the actual failure is will help guide the troubleshooter to get to the root cause of the defect.

So, assuming the material set is as is and the board construction is as is, let's first describe the defect and work through the troubleshooting process.

Zeroing in on the Problem

As described earlier, several boards failed due to an open detected after solder float. While the operations team wanted to blame the newly installed PTH process, closer inspection of the problem showed that the defect was barrel cracking, not a separation or any other defect related to electroless copper. To study the issue further, the fabricator decided to use IST and

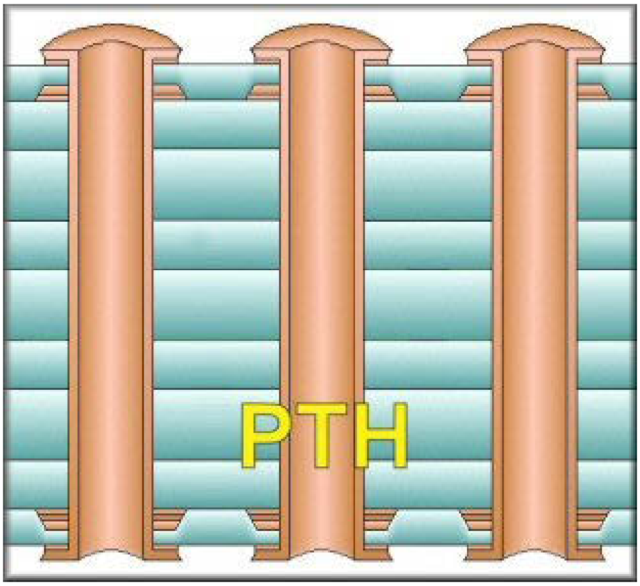


Figure 2: IST coupon GT40800D.
(Source: PWB Interconnect Solutions)

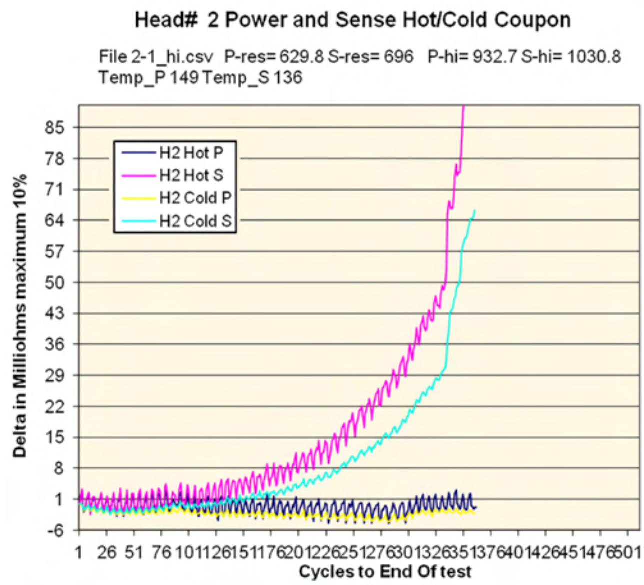


Figure 3: Resistance measurements for the two independent circuits. The "P" is the power circuit–where the direct heat is transferred through the post interconnect and measures change in resistance through the post. The "S" circuit measures the resistance change through the PTH or barrel of the hole. Results for the test vehicle with previous electroless copper.

downloaded the design file. A schematic of the design is shown in Figure 2. Test panels were fabricated as follows:

Stress test (IST) coupon containing plated through-hole technology on a 5.0" (126.9 mm) X 0.7" (17.8 mm) coupon with a total thickness up to and not exceeding 0.125" (3.2 mm) and limited to a minimum of six layers. This coupon is designed on two independent grid sizes, 0.040" (1 mm) and 0.080" (2 mm). The maximum hole/pad size for the .040" (1 mm) grid is 0.015" (.38 mm) drilled and pad size is 0.028" (.7 mm), on both power and sense circuits. The maximum hole/pad size for the .080" (2 mm) grid is .056" (1.42 mm) drilled and pad size is .068" (1.73 mm), on the power circuit.

The test vehicles as described here were built in-house by the fabrica-

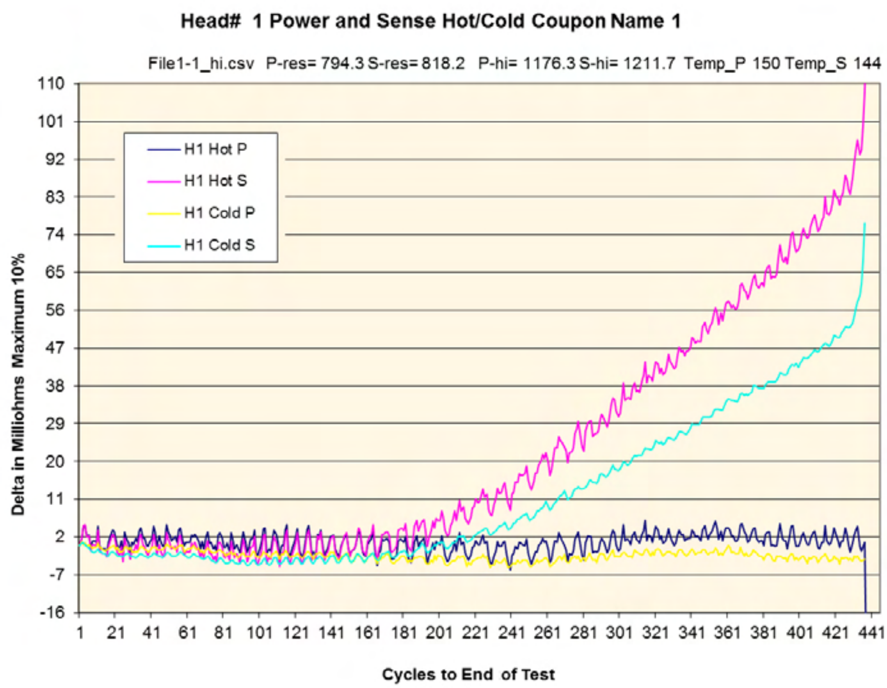


Figure 4: Resistance measurements for the two independent circuits. The "P" is the power circuit–where the direct heat is transferred through the post interconnect and measures change in resistance through the post. The "S" circuit measures the resistance change through the PTH or barrel of the hole. Results for the test vehicle with newer electroless copper.

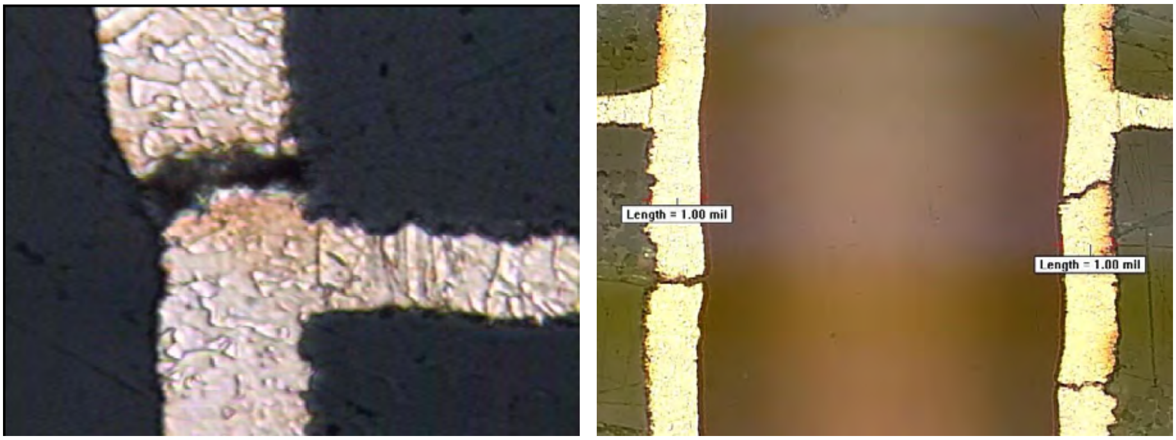


Figure 5: Close-up of PTH cross-section (left); wider view on right. Clearly, barrel cracking is the failure mode.

tor and processed through the facility. One set of panels was processed through the previous electroless copper process. Another set was processed through the new electroless. All other process steps were identical.

Several coupons each were prepared for IST testing. Initial IST results are shown in Figure 3.

Figure 5 shows the results of microsections of the test vehicle coupons after completion of the IST cycles.

As the IST results show, the failure was due to cracking in the PTH (barrel). Note the significant change in resistance detected in the sensing circuit. The power circuit resistance showed little to no change, indicating a robust post connection.

It was clear that the failure in the barrel is related to poor ductility of the acid copper electrodeposit. There was no evidence of undercured resin material that could have partially explained the excessive Z-axis expansion.

Clearly, the root cause of the defect rested within the plated through-hole. If there was significant change in the post interconnect, one could assume that a less than robust electroless copper-to-post interconnection was at least contributing to the failure. But in this instance, that was not the case. The failure clearly rested within the plated barrel of the via.

Thus, possible failure contributors in the PTH are:

- Low ductility of the electroplated copper due to additive imbalance or contamination of the plating solutions
- Thin electroplated copper in some areas of the via (poor throwing power, rough drilled vias, too low of a current applied)
- Columnar grain structure of the plated copper deposit (yielding a deposit of poor ductility)

To understand the failure hierarchy, it can best be described as follows: If the PTH barrel is robust (or the post interconnect quality is very poor), the inter-plane connection will receive increased/extended levels of strain and thus fail. If the PTH barrel is not robust, the failure mode of barrel cracking will totally dominate the interconnect performance, thus the stresses are not given the opportunity to distribute to the innerlayer copper foil interface to cause microcracks. The data collected and the visuals of the microsection clearly indict the plated barrel as the failure mode.

For the engineer reading the resistance graph and using the quantitative data of cycles to failure, insight on the failure mode can be gained. It is critical that the actual failure mode is identified. **PCB007**

References

1. More information on IST can be found by clicking here.
2. IPC-TM-650,2-6-26A.

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.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Lean Challenges: Standard vs. Non-Standard Products

The PCB Norsemen
by Didrick Beck, ELMATICA

People tend to treat standard and non-standard products in the same way; however, they represent two parallel product segments and consequently different challenges for your Lean manufacturing process, especially in relation to production and logistical operations. When you fail to differentiate the processing of standard and non-standard products, not only is the Lean manufacturing process disrupted, but you also introduce a variety of production, financial and logistical challenges. Why take the risk when you don't have to?

Supply Chain Programs

Supply chain programs are designed to decrease inventory, space requirements, lead time and potential quality defects. These programs focus on standardized products as their supply chain can be optimized to increase flexibility, theoretically reduce costs, and increase credit terms, or as some might argue, transfer credit risk to the supplier.

Literature states that these programs are specifically designed to address standardized products[1]. Non-standard products are described as articles, which are customer-unique and designed for a specific purpose[2] (e.g., PCBs and metal casing in the electronic industry).

A supply chain program designed to handle these parallel product segments will consequently fail, because you are trying to "open two locks with one key at the same time." If the aim is to solve the challenges described, you should begin by understanding the capability and goal of the supply chain program and consequently what it is not able to handle, which will be non-standardized products.

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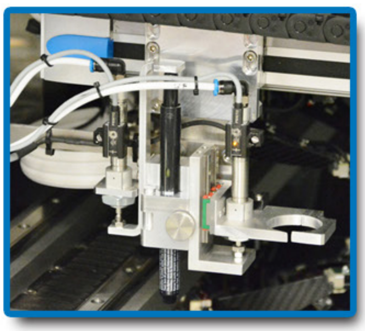

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What program have you selected?

Let's look at different supply chain programs and their methodological framework.

Lean Manufacturing

Lean manufacturing is focused on preserving value with less work. The focus is on reduction of the original Toyota seven wastes to improve overall customer value, but there are varying perspectives on how this is best achieved. Two aspects include:

Reduction of time: Reducing the time it takes to finish an activity from start to finish is one of the most effective ways to eliminate waste and lower costs.

Reduction of total costs: To minimize cost, a company must produce only to customer demand. Over-production increases a company's inventory costs because of storage needs[3].

Just in Time

Just in Time (JIT) is a production strategy that strives to improve return on investment by reducing in-process inventory and associated carrying costs. To meet JIT objectives, the process relies on signals (Kanban) between different points that are involved in the process and tell production when to make the next part. JIT focuses on continuous improvement and can improve a manufacturing organization's return on investment, quality, and efficiency. To achieve continuous improvement, key areas of focus could be flow, employee involvement, and quality[4].

Kanban

This is a method for managing knowledge with an emphasis on JIT delivery while not overloading the team members. In this approach, the process, from definition of a task, to delivery, to the customer, is displayed for participants to see as team members pull work from a queue[5].

Consignment Stock

With consignment stock, a supplier places its stock in the customer's warehouse and the ownership of the consignment stock is passed to the customer when the stock is used (issued or sold in the case of a shop). Unused stock in a warehouse may be returned to the supplier when it concerns standard manufactured products. With customer-specific items, agreements concerning returning products should be negotiated[6].

Continuous Replenishment Program (CRP)

CRP includes the same aspect as Lean manufacturing from the perspective of warehousing and handling.

Vendor Managed Inventory

With vendor-managed inventory, the buyer of a product (business) provides information to a supplier (supply chain) regarding the sale of a product, and the supplier takes full responsibility for maintaining an agreed inventory of the material, usually at the buyer's consumption location (e.g., a store)[7].

Irrespective of the program selected, you are quickly presented with the same challenge: How can a rigid and homogenous manufacturing process system address non-standardized products that are unique and customer-specific? If the systems are designed for optimization and volume production, does that imply they cannot handle non-standardized products?

Non-Standard Products

Supply chain programs are designed to reduce the impact on inventory, space, lead time and quality defects. These elements are analysed here and demonstrate that this is not applicable for non-standard products.

Inventory

Supply chain programs focus on the idea of a small stock with continuous replenishment of orders, often divided into a staged warehouse. As soon as your demand for production increases or decreases, you adjust the current and planned orders, making sure the inventory stays at a minimum. Even though you lose out on the advantage of placing volume orders and you will probably get some upset suppliers, you still end up saving money. Or do you? Studies show that your suppliers will start to adapt to this kind of order frequency and changes, increasing your price. Is JIT a good choice for non-standard products (made-for-order product)?

- Continuous replenishment of stock will consequently also increase handling and transportation costs for all parties.
- Most buyers will seek to reduce their inventory, as inventory equals costs when cash flow is tied up in the warehouse. Accounting and logistic departments are knowledgeable in this respect and seek to continuously reduce the inventory. However, do you compare the price of credit compared to volume orders! Remember if you ask your supplier to hold the stock he will also have to adjust to this reality and in the medium to long run increase the price.

Space

Most non-standardized products (e.g., PCBs) require very little space and should not be a challenge regarding space. Many customers' unique products also have a shelf life and consequently storage time can be a limitation. Hence, these products should optimally be produced to order.

Lead Time

Lead time will be reduced by these supply chain agreements. However, this reduction is dependent upon at least one party taking the extra cost of increased credit terms as the products are invoiced, according to consumption in these programs. There is no reason to store non-standard products in a central storage for dispersal to several customers, because demand is customer unique. This implies that somebody has to be responsible for the increase or decrease in demand and consequently the cost!

Potential Quality Defects

The quality defect ratio for non-standard products and supply chain programs will, in practice, be equal to normal deliveries, hence there is no evidence of quality improvement from employing these programs for custom products. However, these programs will increase the price of quality handling as defects will affect a wide array of complex processes in the supply chain such as storage, communication and transportation. Complex and customer-specific products have more defects than standardized products. For example, if a non-standard product is transported by sea and a quality defect is detected during assembly, the consequence will be significant with respect to new production (unique product), transportation, and assembly.

What is the solution for non-standard products and Lean manufacturing?

As demonstrated, the four goals of supply chain programs are not applicable to non-standard products. The question is, how do we address the two elements these programs aim to achieve, namely, increased flexibility and credit terms?

The question is, how do we address the two elements these programs aim to achieve, namely, increased flexibility and credit terms?

How do we reach the goal of increased flexibility and credit terms at minimum cost? Be sure to set minimum and maximum stock, a large minimum yearly demand to ensure that no small products are subject to the supply chain program, and analyse parameters regarding shelf life and maximum time in warehouse. This will allow for the implementation of automatic invoicing to reduce communication, since time is money.

Only consider non-standardized products for Lean manufacturing processes where you can provide the supplier with binding and adequate weeks forecast. This will allow the supplier to adjust the production volume and transportation method and hence meet the customer's demand and deliver new boards in time if there is a quality defect.

When these parameters are set, it's simple to determine the total credit exposure for the supplier and see this in relation to the general credit terms given to the customer. If this is not analysed, then the credit terms can quickly reach more than 120 days. This is not optimal for any party and it can lead to cash challenges for the supplier, delivering custom products to you, and hence, not easily replaceable if they cannot or are not willing to deliver.

By understanding, discussing and agreeing to the exposure of both parties, namely for the buyer to provide a binding forecast and the supplier to have the correct credit terms, you can then establish an equilibrium situation that is optimal and favourable for both parties, and a non-standardized product can be successfully handled in a Lean manufacturing process.

Implementing non-standardized products in a Lean manufacturing process is hence successful if we avoid normal, non-optimal customer and supplier relationships and focus on a partner-oriented approach where information and liability sharing represents the basis for cooperation. **PCB007**

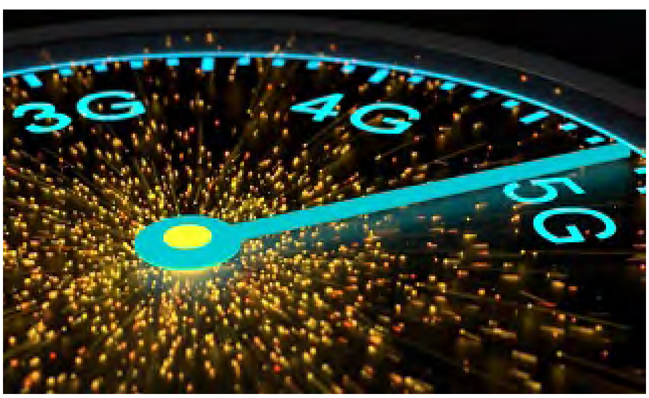
References

1. www.halfcostproducts.com
2. www.mbaskool.com
3. Wikipedia: Lean manufacturing
4. Wikipedia: Just In Time (business)
5. Wikipedia: Kanban (development)
6. Wikipedia: Consignment Stock
7. Wikipedia: Vendor Managed Inventory

Didrick Beck is CEO of Elmatica.

Flexible and Dynamic Transport Solution for Future 5G Communications Developed

The 5G-Crosshaul consortium was selected in 2015 to develop a 5G transport network that would integrate backhaul and fronthaul, two typical segments of the 4G telecommunications networks. On the fifth generation of communication networks that is expected to replace 4G around 2020, these two segments merge into what is known as crosshaul, to enable a flexible and software-defined reconfiguration of all networking elements in a multi-tenant, service-oriented and unified management environment.



The transport network now presented flexibly interconnects distributed 5G radio access and core network functions hosted on in-network cloud nodes. This configuration is achieved through the implementation of a control infrastructure coupled with a unified data plane, encompassing innovative high-capacity transmission technologies as well as novel deterministic-latency switch architectures. "The data plane is like a muscle, while the control infrastructure would be like a brain. Thanks to their integration we can move a huge amount of data in a very short time, and we can do it by controlling how long it takes to perform this process," explains one of the researchers.

"It has been truly an honor to oversee one of the most ambitious 5G transport network research and development efforts to date," said the Coordinator of the 5G-Crosshaul project, Arturo Azcorra, Professor at the Telematics Department of UC3M and Director of IMDEA Networks. "The successful results of the 5G-Crosshaul project have advanced scientific knowledge and the international standardization of 5G systems."

Recent Highlights from PCB007

1 Unimicron Germany Rises from the Ashes with New Smart Factory ▶

This is a review of the grand opening of Unimicron's new smart factory in Geldern, Germany. A fire in a PCB shop is an experience we all dread, but still it happens, and the consequences can be devastating. In the early hours of December 28, 2016, the innerlayer production plant at RUWEL International in Geldern caught fire and the whole factory and its contents were destroyed.

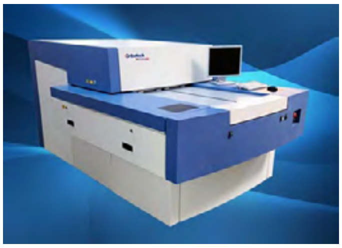
2 Chin-Poon PCB Plant Fire to Affect 15% of Revenues ▶

Chin-Poon Industrial, which has more than 70% of its revenues from the automotive electronics industry, has estimated that losses resulting from a deadly fire at its production site in Taoyuan, Northern Taiwan on the evening of April 28 will amount to about NT$300 million ($10.2 million).

3 Flex Talk: Something New for Everyone ▶

Whether you are new to single- and double-sided flex, moving into rigid-flex construction, thinking of using bookbinder technology, or investigating an additive process, working with new technology can be both exciting and challenging.

4 Printed Circuits Upgrades Photo Department ▶



Flex and rigid-flex circuit board manufacturer Printed Circuits has added two new pieces of equipment to their photo department including a new Orbotech Paragon 8-watt laser direct imager and a Fusion 22 automatic optical inspection machine with laser via inspection capabilities.

5 It's Only Common Sense: Silence is Not Always Golden ▶

A few years ago, I worked with a client that won and then lost 30 customers all in the span of 10 months. They had bought the customer base of a company that was going out of business.

6 The Right Approach: the Rebirth of Made in America ▶

I have been on the record for the past 10 years saying that jobs we lost overseas may move out of China to a new low-cost country, but they were never coming back. I have never been happier to be wrong! I talk to a lot of CEOs, and the first question I ask is, "How's business?" The answers are overwhelmingly positive, and it is clear that their optimism is at a level not seen for over a decade. America as a low-cost country. Think about that.

7 AT&S Offers a Look into the Future of Connection Technology ▶

AT&S presented innovative technologies and trends in connection solutions at the 14th AT&S Technology Forum. Numerous interested customers were able to find out about the latest developments in the electronics and printed circuit board industry for areas such as mobile devices, automotive, industrial, communications and medical technology and to exchange views with the AT&S experts.

8 Nano Dimension Sells Three Printers, Opens Customer Center at U.S. HQ ▶

Nano Dimension Ltd. has announced new sales of the DragonFly 2020 Pro 3D printer to three prominent American customers. Nano Dimension also announced the opening of its third Customer Experience Center co-located with the company's U.S. headquarters in Santa Clara, California.

9 Automotive, the Electronics Industry's New Driver ▶

The automobile industry is becoming a combination of most of the traditional electronics segments: It's a consumer product with a computer, communications center, and a few medical monitoring-type tendencies (measuring your alertness, heart rate, etc.), all rolled (no pun intended) into one incredible machine that is influencing our industry as none other.

10 Varitron Technologies Ramps Up for Commercial Printable Electronics Production ▶

The intelliFLEX Innovation Alliance announced today that Varitron Technologies is joining its eco-system and making a substantial investment to develop its capabilities in flexible and hybrid electronics (FHE).

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Career Opportunities

ZENTECH

Zentech Manufacturing is Hiring Manufacturing Engineers!

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add a Manufacturing Engineer. We offer an excellent benefit package including health/dental insurance and an employer-matched 401k program, and we hold the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485. Zentech is an IPC Trusted Source QML and ITAR registered.

U.S. citizens only need apply.

Please email resume to sales@zentech.com.

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MacDermid Enthone
ELECTRONICS SOLUTIONS

Technical Service Rep, Northeast

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Technical Service Rep will be responsible for day-to-day support for fabricators using MacDermid Enthone's chemical products. The position requires a proactive self-starter who can work closely and independently with customers, sales group members and management to ensure that customer expectations and company interests are served.

- Thoroughly understand the overall PCB business, and specifics in wet processing areas
- Prepare action plans for identification of root cause of customer process issues
- Provide feedback to management regarding performance
- Create and conduct customer technical presentations
- Develop technical strategy for customers
- Possess the ability to calm difficult situations with customers, initiate a step by step plan, and involve other technical help quickly to find resolution

Hiring Profile

- Bachelor's Degree or 5-7 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Extensive experience in all aspects of customer relationship management
- Willingness to travel

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Career Opportunities

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "U.S. Sales Manager—tec-speed" in the subject line.

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PCB Manufacturing, Marketing Engineer

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, tradeshow, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

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Career Opportunities

ventec
INTERNATIONAL GROUP
騰輝電子

Technical Support Engineer, UK

As a UK-based Technical Support Engineer, you will help customers choose and optimize the use of Ventec materials in their Printed Circuit Board manufacturing processes. You will provide a two-way channel of technical communication between Ventec's production facilities and UK/European customers. You will be required to undertake some laboratory testing (including the use of TMA, DSC, Melt Viscometer, Gel Plate Timer, and laboratory scale multilayer presses) and provide appropriate technical support to Ventec UK and European sales personnel to maximize results.

Skills and abilities required for the role:

- Hold a HNC, HND, degree or equivalent in a technical/scientific discipline.
- Excellent communications skills and ability to write full technical reports for group or customer distribution.
- Ability to work in an organized, proactive, and enthusiastic way.
- Ability to work well, both in a team as well as an individual.
- Good user knowledge of common Microsoft Office programs.
- Full driving license essential.

Appropriate training will be given if required.

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. For more information, please click here.

Please forward your resume to HR@ventec-europe.com.

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BLACKFOX®
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Events Calendar

IMS 2018 International Microwave Symposium ▶
June 10–15, 2018
Philadelphia, Pennsylvania, USA

Eurosatory 2018 Defense and Security International Exhibition ▶
June 11–15, 2018
Paris, France

IPC E-Textiles 2018 Workshop ▶
September 13, 2018
Des Plaines, IL, USA

electronica India productronica India ▶
September 26–28, 2018
Bengaluru, India

electronicAsia 2018 ▶
October 13–16, 2018
Hong Kong

SMTA International ▶
October 16–17, 2018
Rosemont, Illinois, USA

TPCA Show 2018 ▶
October 24–26, 2018
Taipei, Taiwan

electronica 2018 ▶
November 13–16, 2018
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair ▶
December 5–7, 2018
Shenzhen, China

Additional Event Calendars

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